# DIFFERENT APPROACHES ON SEU MITIGATION TECHNIQUES FOR PLDS

MASTER's THESIS

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# ABSTRACT

The use of FPGAs in commercial systems is nowadays more than normalize due their great configurability. The possibility of achieving complex logic duties with the use of a unique device added to their intrinsic reusable capabilities, make these devices a high valuable choice for electronics designers. These values are not passing in vain in the space community that started using FPGAs for non critical systems ten years ago. However the use of configurable devices in harsh environments is not near as established as it is on commercials or industrial systems.

Up to day, only the so called antifused technology FPGAs are qualified for radiation environments. These FPGA are guaranteed up to a reasonable level of radiation to operate as they will do without the effects of high energetic particles. However these FPGA have two main disadvantage when comparing with SRAM based ones; firstly and most important, these are One Time Programmable (OTP) devices that once they are programmed, is not possible to change their behavioral; also new generation re-configurable FPGA, as the ones from Xilinx, have really high value embedded modules as hard-processors, multipliers, memories and Digital Signal Processors (DSPs). Although Xilinx and other SRAM FPGAs manufactures had performed great efforts to mitigate the radiation on theirs devices, achieving Total Ionizing Dose (TID) and Single Even Latch-Up (SEL) immunity, Single Event Upsets (SEU) are still a failure point on SRAM configuration memories.

The aim of this master's thesis is to cover the lack of up to day technology resolving SEUs. The idea is to use a radiation tolerant reconfigurable device, and design systems to mitigate the effects of SEU, removing single points of failure. This master's thesis proposes two different ways of achieving a Rad-Hard by design system using redundancy, along with other techniques, at two key levels. Firstly, a complete SoC protected with new XTMR (Triple Module Redundancy) for SEU mitigation, along with a self scrubber module used for avoiding cumulative errors in configuration memory, is presented. This module will take advance of typical non-volatile memories used in On-Board Computers (OBC) to allow in mission self reconfiguration without interfering in OBC to memory communications. The second proposal is a device level redundancy where the lack of immunity of each device is assumed by a distributed architecture where critical duties are always performed by at least three devices at a time.

Therefore, one mitigation scheme is proposed at tow different levels. First approach uses logic redundancy inside one device to mitigate the effects of radiation, while the second approach takes advantage of a distributed device architecture to discard erroneous parts and assure the healthiness at a system level.

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# 0 ACRONYMS

| | |
|---|---|
| **AIT** | Assembly, Integration and Test |
| **BER** | Bit Error Rate |
| **BW** | Band Width |
| **CAN** | Control Area Network |
| **COTS** | Commercial Off The Shelf |
| **CPLD** | Complex Programmable Logic Device |
| **DOT** | Distributed OBDH Terminal |
| **EGSE** | Electrical Ground Support Equipment |
| **EPH** | Enhanced Processing Hardware |
| **FPGA** | Field Programmable Gate Array |
| **FSM** | Finite State Machine |
| **Gbps** | Gigabit per second |
| **H/K** | House Keeping |
| **H/W** | Hardware |
| **ICAP** | Internal Configuration Access Port |
| **I/F** | Interface |
| **JPL** | Jet Propulsion Lab |
| **kbps** | kilobit per second |
| **LEO** | Low Earth Orbit |
| **Mbps** | Megabit per second |
| **MTBFF** | Mid Time Before Functional Failure |
| **n.a.** | Not Applicable |
| **OBC** | On Board Computer |
| **OBDH** | On Board Data Handling |
| **OWLS** | Optical Wireless Links for intra-Satellite communications |
| **PCB** | Printed Circuit Board |
| **PDU** | Power Distribution Unit |
| **P/L** | PayLoad |
| **PLD** | Programmable Logic Device |
| **QOS** | Quality Of Service |
| **RTU** | Remote Terminal Unit |
| **S/C** | Spacecraft |
| **SEE** | Single Event Effects |
| **SEL** | Single Event Lath-up |
| **SEFI** | Single Event Functional Interrupt |
| **SEU** | Single Event Upset |
| **SoC** | System on Chip |
| **S/S** | Sub-System |
| **S/W** | Software |
| **TBC** | To be confirmed |
| **TBD** | To be defines |
| **TC** | Telecommand |
| **TID** | Total Ionizing Dose |
| **TM** | Telemetry |
| **TTC** | Telemetry Tracking and Command. |
| **UART** | Universal Asynchronous Receiver-Transmitter |
| **VHDL** | Very High Level Description Language |

# 1 INTRODUCTION

The capacity and performance of FPGAs suitable for space flight have been increasing steadily for more than a decade. In reprogrammable devices the increase has been from tens of thousands to millions system gates. The application of FPGAs has moved from simple glue logic to complete subsystem platforms that combine several real time system functions on a single chip, even including embedded microprocessors and memories [TIG01], [CON99]. The potential for FPGA use in space is continuously increasing, opening up new application areas. The FPGAs are more commonly being used in critical applications and are replacing ASICs on a regular basis.

The behavioral of electronics components may be altered under space radiation. There are several phenomena that will be described here after that may cause transient malfunctioning and also part's failure. Even though new generation FPGAs has been manufactured with radiation tolerance, still memory configuration and logic registers are susceptible to Single Event Effects that may provoke errors on the functionality implemented. Prior to decide a mitigation technique to be applied to the design, it's very important to analyze the requirements of the mission in which the FPGA system will be involved. If the FPGA is to be deployed on a space critical mission in harsh environment, the mitigation scheme should involve redundant FPGA with configuration management. In the other side, application such image capture where operating window is small, no mitigation scheme may be applied. In between these two opposite scenarios there are several mitigations schemes that may fulfill our mission requirements. The following chart shows an overview for mitigation scheme selection based on the application and environmental needs proposed by Xilinx on [BRE08-a]:

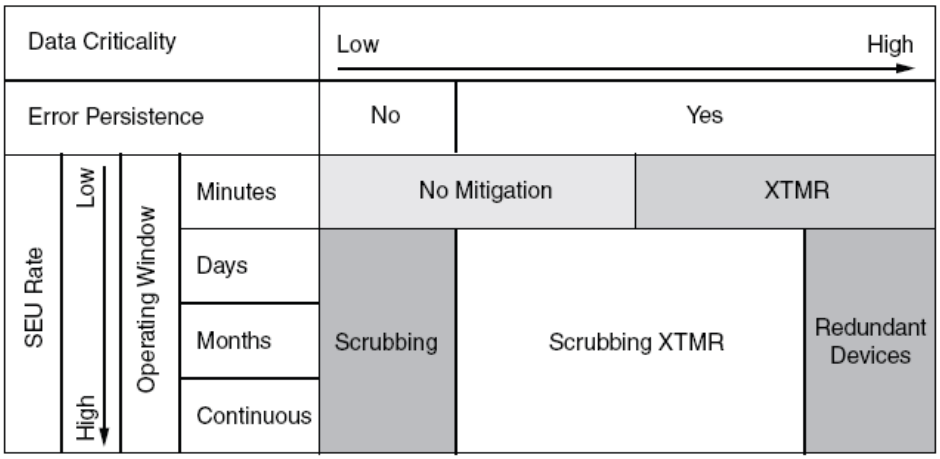


**Figure 1: Mitigation Scheme Matrix proposed by Xilinx.**

Mitigation techniques are being applied already to duplicate and triplicate the hardware modules (TMR), in order to be able to detect and correct this error on real time. However also configuration memory must be treated in order to avoid cumulative SEU in it, invalidating the other mitigation techniques. As will be described here after, memory configuration may be readback and compare with original from an external ROM. If any error is found, then it is possible to re-write the bitstream into the configuration memory without halting the FPGA running process. When doing this continuously and cyclically it is called scrubbing [CAR00]. Thus when designing electronics systems to run at space level, several considerations must be taken into account in order to assure its own healthiness.

This Master's Thesis will review radiation effects that may alter reconfigurable FPGAs function, and then several solution approaches will be expose in order to mitigate the effect of radiation particles inside FPGAs.

## 1.1 MOTIVATION

The use of FPGAs in high-radiation environments is not yet well accepted by many people inside the space market [WAL01], but there is an increasing interest in these devices due to the improved cost efficiency and the lower development time in comparison to other design options such as ASICs or discrete logic. Also advent of reprogrammable devices featuring millions system gates, it is not longer feasible to disregard these technologies.
Another important advantage of SRAM-based FPGAs is their capability of being in-system reconfigured. This feature is especially important in space applications, because it allows modifying on-board hardware by replacing faulty/outdated FPGA bitstreams at different stages of a mission [BRO01]. Some example uses are: rectification of design faults, improvement of processing algorithms, alteration of system functionality in response to changed mission requirements, modification of hardware configurations to reduce power characteristics, etc.

## 1.2 APPROACH

Different approaches are proposed for different situations. A first one device approach is considered for typical On-Board Data Handling units where a unique processor is used for all on-board management capabilities. In this approach, an XTMR system along with continues self readback/scrubbing cycles is proposed. The novelty of this approach is to reduce the hardware needs in terms of an external Rad-Hard configuration manager. An internal IP Core takes advantage of typical ROM devices used in these instruments, and coordinates the mitigation technique with processor's memory access.

A different approach is proposed for systems with distributed capabilities. The second proposal, assumes that the devices to be used will not be able to mitigate radiation failures induced by SEUs for the whole mission. Therefore, a redundant distributed processing with triplicated voters will be able to detect those errors and also keep the healthiness of the results for typical critical duties. For this solution COTS has been used. These COTS have been precisely qualified with a proton irradiation campaign to assure TID and SEL immunity up to reliable levels. These tests are also reported.

## 1.3 OBJECTIVES

The objective of this master project is to find innovative designs alternatives for mitigating the effect of radiation on PLDs, and also evaluate future uses of this technology within spacecrafts and artificial satellites.

## 1.4 THESIS' ORGANIZATION

This document is divided in seven chapters. First three chapters introduce the basic concepts related to radiation effects on PLDs as well as the state of art of mitigating techniques nowadays. Chapters fourth and sixth describe the innovative ideas presented by the author to

improve system reliability when using Xilinx FPGA in a harness space situation. The fifth chapter explains the results obtained from a proton irradiation campaign done over CoolRunner-II Xilinx CPLD to evaluate its tolerance to Single Event Latch-Ups and Single Event Upsets. This CPLD where selected due to its ultra low power consumption to be used on small satellites or self-powered sensor. Finally, chapter seven will discuss the results found through this master's project and the main guidelines to follow in the near future.

# 2 RADIATION EFFECTS

## 2.1 SPACE ENVIRONMENT

It is important to know which the space environment is where spacecrafts and satellites will be operating. There are high-energy particles that will irradiate hardware provoking malfunctions and even permanent damage into electronic components inside. These high-energy particles are mainly divided in three categories. The first is particles trapped by planetary magnetic fields such as the earth's Van Allen Belts. The second is the comparatively low-level flux of ions that originate outside of our solar system called galactic cosmic rays. The third is bursts of radiation emitted by the sun, characterized by high fluxes of protons and heavy ions, referred to as solar particle events.

### 2.1.1 Trapped Particles

The radiation belt trapped radiation environment includes protons with energies up to several hundred MeV, and two electron belts, whose spectrum extends to energies of a few MeV. The combination of their motions in the Earth's magnetic field (gyration about field lines, bouncing between the magnetic mirrors, and drift around the Earth) makes the particle field at the spacecraft effectively isotropic [REE00].

In the following figure, a representation of the Van Allen Belts and particles trapped inside may be observed:

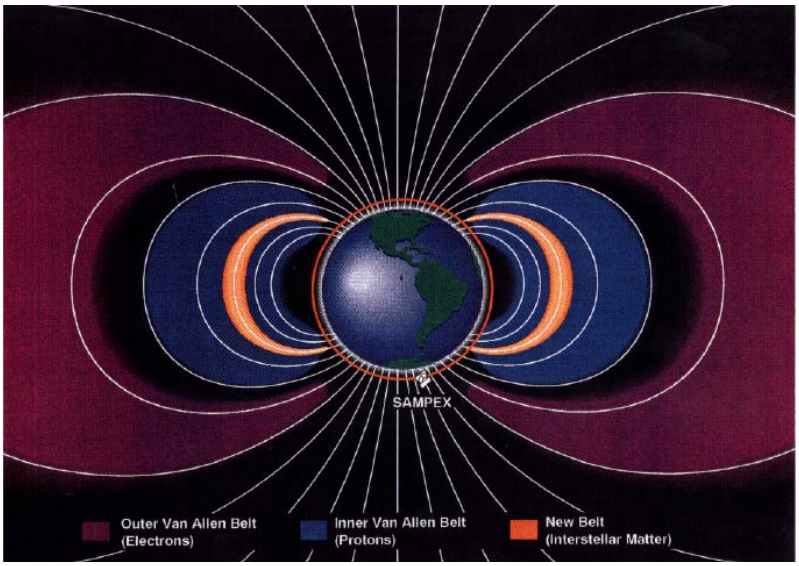


**Figure 2: Location of a radiation belt (shown in orange) whose ultimate source is material from the local interstellar medium.**

Trapped proton energies extend up to a few hundreds of MeV, at which point the fluxes begin to fall off rapidly. The energetic trapped proton population with energies greater than 10 MeV is confined to altitudes below 20,000 km, while protons with energies of about 1 MeV or less are observed at geosynchronous altitudes and beyond.
Trapped protons can cause Total Ionizing Dose (TID) effects, Displacement Damage DD) effects and Single Event Effects (SEE). The metric used for TID studies is ionizing dose,

defined as the energy deposited per unit mass of material that comprises the sensitive volume. The unit commonly employed is the "rad" where 1 rad = 100 erg/g.

There are two areas where trapped electrons are situated, in the inner zone and in the belt. In the inner zone electron energies range up to approximately 4.5 MeV. The flux value is about 106 cm-2s-1 for energies above 1 MeV electrons. These fluxes gradually increase during solar maximum by a factor of 2 to 3. In the outer zone (or belt) electron energies are generally less than approximately 10 MeV. Here the long-term average value for energies above 1 MeV electrons is roughly 3 x $10^6$ $cm^{-2}s^{-1}$. This zone is very dynamic and the fluxes can vary by orders of magnitude from day to day.

### 2.1.2 Galactic Cosmic Rays

Galactic cosmic rays (GCR) are high-energy charged particles that originate outside of our solar system and are believed to be remnants from supernova explosions. All naturally occurring elements in the Periodic Table (up through uranium) are present in GCR, although there is a steep drop-off for atomic numbers higher than iron (Z=26). Energies can be as high as 1000 GeV, although the acceleration mechanisms to reach such high energies are not understood. Fluxes are generally a few per $cm^{-2}s^{-1}$, and vary with the solar cycle [XAP06-a]. SEE are the main radiation effects caused by GCR in microelectronics and photonics. The metric traditionally used to describe heavy ion induced SEE is linear energy transfer (LET).

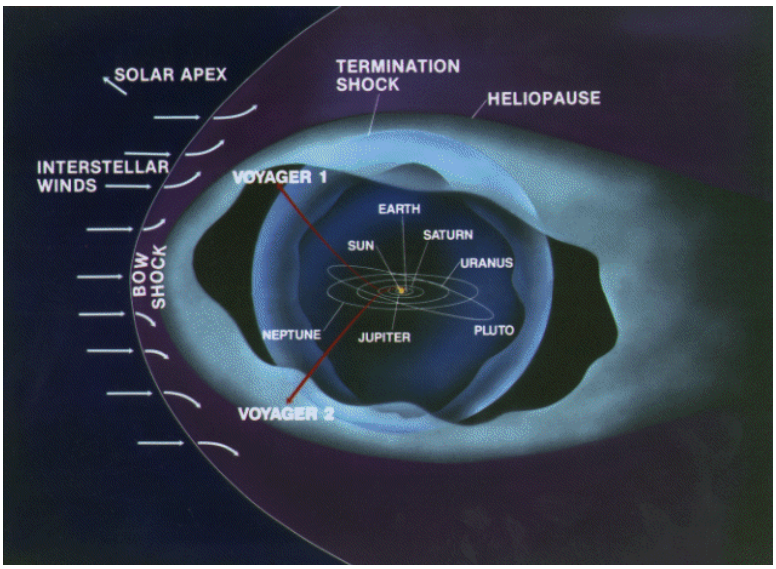


**Figure 3: Heliosphere cartoon with GCR entering into our Solar System.**

### 2.1.3 Solar Particle Events

It is believed that there are two categories of solar particle events and that each one accelerates particles in a distinct manner. Solar flares result when the localized energy storage in the coronal magnetic field becomes too great and causes a burst of energy to be released. They tend to be electron rich, last for hours. Coronal Mass Ejection (CME), on the other hand, is a large eruption of plasma (a gas of free ions and electrons) that drives a shock wave outward and accelerates particles. CMEs tend to be proton rich and last for days [REA99].

All naturally occurring chemical elements ranging from protons to uranium are present in solar particle events. They can cause permanent damage such as TID and DD that is due mainly to the proton and possibly gamma component. Just because the heavy ion content is a small percentage does not mean it can be ignored.

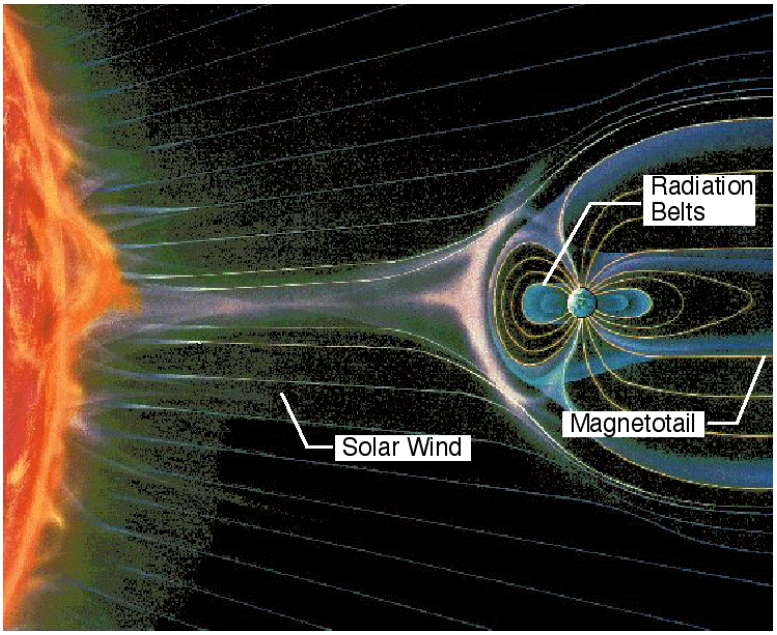


**Figure 4: Sketch of the Earth's magnetosphere and its interaction with the solar wind.**

The sun is both a source and a modulator of space radiations. Understanding its cyclical activity is an important aspect of modeling the space radiation environment. The solar activity cycle is approximately 11 years long. During this period there are typically 7 years during solar maximum when activity levels are high and 4 years during solar minimum when activity levels are low. In reality the transition between solar maximum and solar minimum is a continuous one but it is often considered to be abrupt for convenience. At the end of each 11-year cycle the magnetic polarity of the sun reverses and another 11-year cycle follows. Thus, strictly speaking the total activity cycle is approximately 22 years long. Magnetic polarity apparently only affects the galactic cosmic ray fluxes [BAD96], and not the trapped particle or solar particle event fluxes. Thus, things are often viewed on an approximately 11-year cyclical basis.

Solar particle events are known to occur with greater frequency and intensity during the declining phase of solar maximum [SHE95]. Trapped electron fluxes also tend to be higher during the declining phase [BOS03]. Trapped proton fluxes in low earth orbit (LEO) reach their maximum during solar minimum but exactly when this peak is reached depends on the particular location [HUS98]. Galactic cosmic ray fluxes are also at a maximum during solar minimum but in addition depend on the magnetic polarity of the sun [BAD96].

To conclude this subsection, the following figure represents in a simplified manner the particle spectra of the near Earth space environment [XAP06-b]:

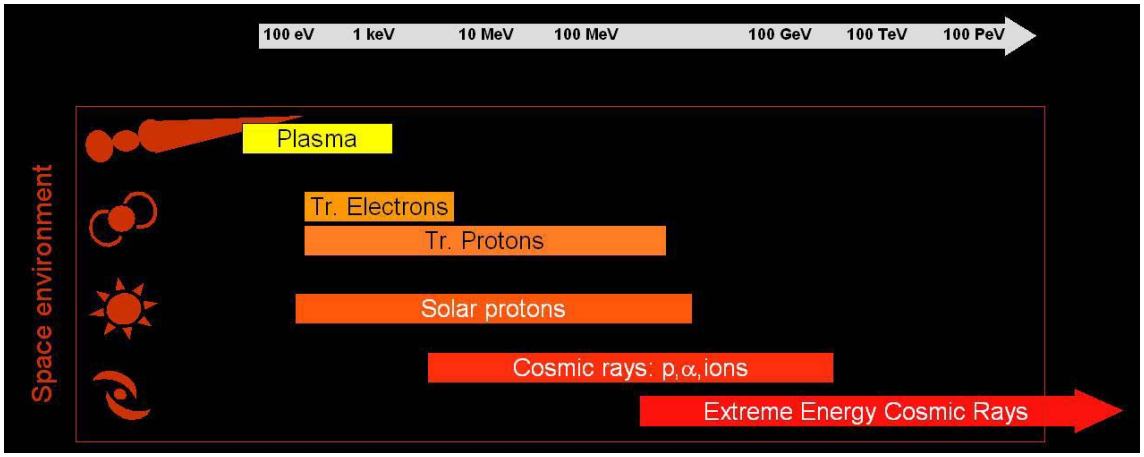


**Figure 5: Simplified diagram of typical particle radiation spectra.**

## 2.2 RADIATION EFFECTS ON ELECTRONICS

In this section the interaction of space environment particles with electronics will be described.

In the interaction of energetic heavy ions with matter, the energy is primarily transferred to target electrons. The high energy primary electrons (also called gamma rays) decay in an electronic cascade, and finally produce dense plasma of electron hole pairs. When measuring the heavy ion capacity to produce damage to a semiconductor, we talk about LET, which is the energy lost by the ionizing particle per unit path length in the sensitive volume. The units of LET that are commonly used are then MeV-cm$^2$/mg.

Unlike heavy ions induced SEE, proton-induced SEE occur as a result of target recoil products that result from interactions with the incident proton. The incident proton energy has a significant influence on these products and that is the reason why results are commonly presented in terms of it.

SEE are quite different to total dose radiation which causes gradual global degradation of device parameters and dose-rate radiation which causes photocurrents in every junction of a circuit. A single event interaction is a very localized effect, and can lead to a seemingly spontaneous transient within a region of the circuit.

Heavy ions, as well as protons and alpha particles in solar particle events, can cause static, transient and permanent SEE. Find below a brief description on the most typical Single Event Effects:

- **Single Event Latch-up (SEL)** is a condition where the parasitic pnpn structure in CMOS is latched to a high current state. This can either be destructive or non-destructive. In the non-destructive case, the affected device will have to have power recycled to restore normal operation. Long term high current will eventually result in failure.

- **Single Event Transient (SET)** is the physical signal glitch caused by an SEE. This effect does not persist in time, however depending if it hits a combinational logic or a memory cell, it may propagate the error to other parts of the device.

- **Single Event Upset (SEU)** is a bit flip or other corruption of stored information due to an SEE (usually applied to memory circuits).

- **Multiple Bit Upset (MBU)** is a SEE that affects multiple circuits at once, not from multiple ion/proton hits but from one event. This is seen in memory cells where many nodes that are physically adjacent are affected (spatial relationship). It is also seen in sequential circuits operating at a high rate of speed, much faster than the single event, so that multiple clocked bits are errant (temporal relationship).

- **Single Event Functional Interrupt (SEFI)** is an SEE that affects a critical portion of the circuit design, like a state machine. A SEFI is non-destructive, but may linger for a long time causing incorrect operation of the circuit. An example is a SEU in the power-on reset circuit that initiates a reset while the circuit is operational.

# 3 STATE OF ART

We will start this section reviewing the different mitigation techniques that have been developed for configurable devices. Then a review the up to date studies performed over Xilinx FPGAs in terms of radiation sensibility over the different events studied on the previous section. Also a break down of the susceptible parts of the FPGA architecture will be reviewed and which techniques have been applied to mitigate them.

A lot of test at proton and heavy ions radiation facilities has been performed to find out the behavioral of these devices under harnessing environment. These tests will also be discussed here after.

## 3.1 MITIGATION TECHNIQUES

Mitigation techniques are well separated in two mayor groups. The ones so called technological techniques are based on changing at physical level the configuration of the hardware it self, or changing the manufacturing process to build more robust hardware against radiation. Devices manufacture in such a way, are called Rad-Hard parts. This term means that are immune to TID, SEL and SEU up to given values. These processes are very expensive in compare with typical commercial ones. However, it isn't only an economic matter. Even though technological processes have performed great advantages on this area, so has done or even more in the commercial ones, allowing electronic devices achieve speed marks not easily achieved with manufacture changes.

The second group of mitigation techniques is applied at higher levels. These techniques are called hardening techniques, and seek for achieving Rad-Hard by design devices that are only Rad-Tolerant by manufacture. Rad-Tolerant devices are those which are immune to TID and SEL but not to SEU. This is the case of study of this master's thesis. Most techniques used consist on applying redundant information in such a way that allows to detect or correct the errors induced by SEU in the memory or combinational elements. Depending on its nature, these techniques may be separated in two groups:

### 3.1.1 Hardware Redundancy

These techniques shall replicate the logic blocks in the circuit in such a way that the same duty is performed several times at a time. The most popular consist in replicate N-times the block (where N is always an odd number) that shall be hardened and use a majority voter at the output to choose the correct one. This technique is named NMR (N Module Redundancy) and the most common application of it is TMR (Triple Module Redundancy), where the module is replicated three times and the method may detect and correct any single upset. The following caption shows a typical module with and without triple redundancy:

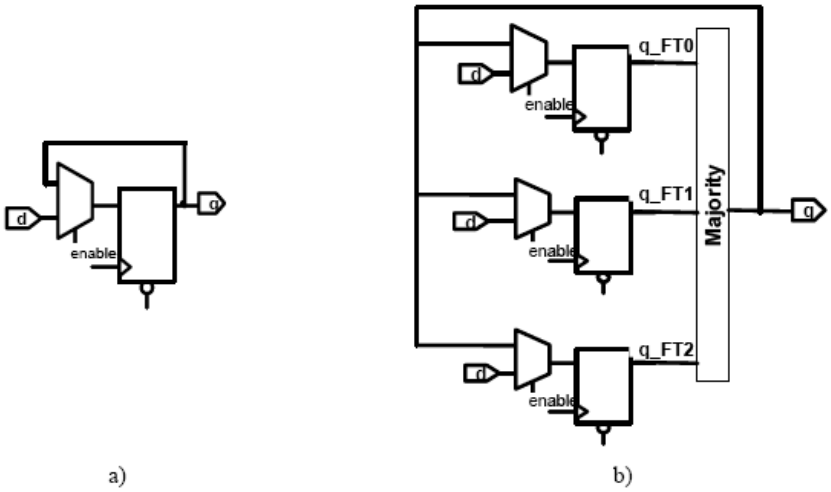


**Figure 6: figure 'a' represents the original module and 'b' the TMR one.**

This technique has three problems on its application. First of all, it will work for single errors but not for multiple errors. Also a hit in the voter's output will not only propagate the error to 'q' but also will feed the inputs with erroneous data. First two are independent of the device used, however, when applying this inside reconfigurable FPGAs a third problem is encountered. Even though flip flop registers is protected, configuration memory that configures and interconnects everything inside the FPGA may be hit as well, and therefore SEU errors may accumulate causing the module to fail. In order to solve this problem, scrubbing cycles are recommended. These scrubbing cycles will correct the single event bit flips in configuration memory without interrupting the running process.

Also Xilinx has developed an improved TMR method, called Xilinx TMR (XTMR). Unlike traditional TMR, the XTMR approach involves [XIL07]:

- Triplicating all inputs including clocks and throughput (combinational) logia.
- Triplicating feedback logic and inserting majority voters on feedback paths.
- Triplicating all outputs, using minority voters to detect and disable incorrect output paths

All these improvements protect against SEU in voting logic as well as SET. Also triplicating the IO Blocks avoid failures in the output circuit of the FPGA. However this method increases by a factor of 3.2 to 5.6 the used logic depending on the design [XTM08-b].

The following figure shows an XTMR module:

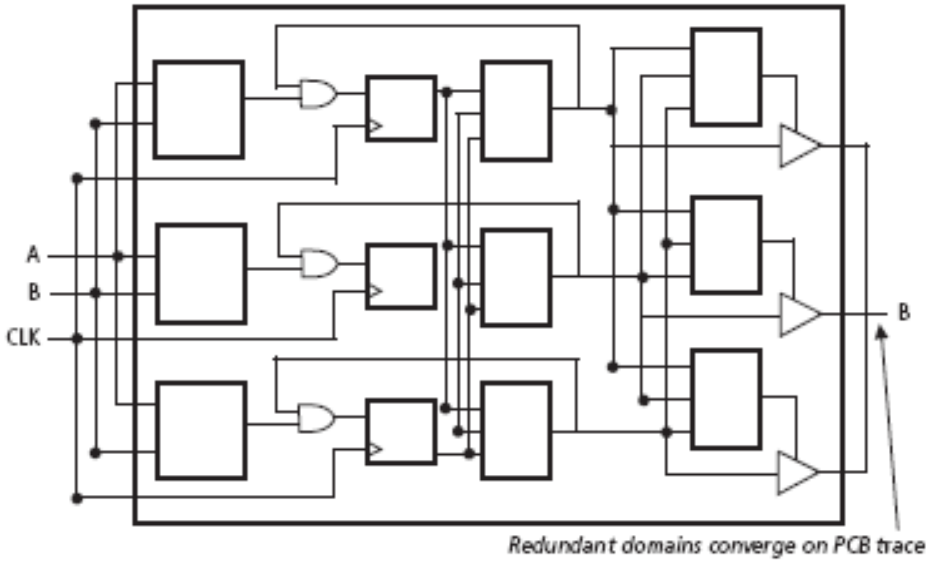


**Figure 7: Module hardened by XTMR method.**

### 3.1.2 Information Redundancy

The transmitted information by an electronic device may be a serial concatenation of '1' and '0'. If in this transmitted message a bit flip is produce a valid but erroneous data may be acknowledged. To avoid this situation there are several methods that adding some extra information may be able to detect and even correct errors on the message. In the next paragraphs will be described the most common information redundancy techniques.

#### 3.1.2.1 Parity Codes

These are most simple codes consisting in adding a parity bit at the end of the transmission. This bit will indicate if the number of '1's or '0's is odd or even. This code has the property of detecting any odd number of errors in the sent frame.

#### 3.1.2.2 Error Correction. Hamming

As explained at [POR07], this codes are extension of parity codes, where to correct n bits, another i bits are added. The number of bits added is given by the formula:

$$2^i \geq i + n + 1$$

The original message is divided in groups and for each group a parity bit is added. For example for the message "n3, n2, n1, n0", three parity bits are needed, "i1, i2, i3". The information bits are divided in three groups and a parity bit is calculated: (n3, n2, n1, i3), (n3, n2, n0, i2), (n3, n1, n0, i1). Thus if there is an error on n3, the three parity bits will indicate the error, if n2 is the erroneous bit, parity bits i3 and i2 will indicate the error, and so on.

Error Correction Codes (ECC) are the most common methods for correcting errors on memories [NIC05], especially on SRAM ones which are usually more susceptible to SEUs.

## 3.2 SUSCEPTIBILITY MEASUREMENT METHODS

When trying to measure the FPGA susceptibility it's completely necessary to implement two different methods. Single Event Upsets (SEU) may alter the logic state of any static memory

element. Since the user-programmed functionality of an FPGA depends on the data stored in millions of configuration latches within the device, an SEU in the configuration memory array may have adverse effects on the expected functionality.
Although, a static upset in the configuration memory is not synonymous of a functional error. Upsets may have no effect on functionality. This is due to not all configuration bits will affect in the specific design. A typical scenario where SEU may not alter the FPGA functionality is as shown in [XTM08-a]:

- A SEU hit a CMC that controls unused routing (statistically this is the most likely scenario).

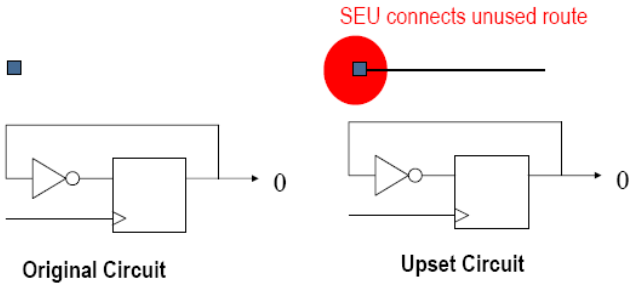


**Figure 8: SEU hit on unused routing.**

The configuration bitstream stores the information about all Lookup Table (LUT) values, CLB, IOB, and BRAM control elements, as well as all interconnect control. Therefore, every programmable element within the FPGA can be addressed with a single read or write operation. All of these configuration latches can be accessed without any disruption to the functioning user design, which means that partial reconfiguration may be used to recover upseted data without stopping the FPGA normal processing.

The second method to be implemented when trying to test the device susceptibility is a dynamic test, where special FPGA features that are not accessible from the configuration bitstream may be tested. On [SWI05], special care was taken to test Digital Clock Manager (DCM) and IO Blocks from Virtex-II. Also BRAMs and embedded multiplier were tested.

Dynamic test is not only useful for testing these embedded components but also to measure the effectiveness of the mitigation techniques. Results of these tests will be shown on the following sections.

# 4 RADIATION TEST

In this section we present two different radiation test performed. The first report is for the test performed by the SEE Consortium to Virtex-II FPGA.

A second report of a radiation campaign to CR-II CPLD is presented. This campaign was performed by the author along with his laboratory working at INTA, in collaboration with Universidad Carlos-III de Madrid. A paper presented at RADiation and its Effect on Components and Systems (RADECS) 2008 international conferences and it's attached on Annex 1 [GAR08].

## 4.1 VIRTEX-II TEST

### 4.1.1 SEL AND TID SUSCEPTIBILITY

Single Event Latch-up (SEL) and Total Ionizing Dose (TID) do not present a problem on Xilinx Virtex-II FPGA. The radiation hardened devices are manufactured on a thin epitaxial substrate.

For TID these devices are guaranteed by Method 1019.5 (Dose Rate ~50.0 rad (Si)/sec) up to 200 Krad as shown at this device family data sheet [XDS06].

As shown in [SWI04a], a XQR2V3000-FG676 device was used for these latch-up tests. All experiments were conducted using 15Mev/amu gold ions. The stopping power of the ions was changed by altering the angle of incidence between normal incidence and 60 degrees. The following table summarizes the change in range and stopping power as a function of incident angle. The applied fluxes were typically of an order of magnitude of 105 particles/cm2/s and multiple runs were conducted in order to obtain the total fluences shown.

| Heavy Ion | Angle | Degrader | Effective LET [MeV/mg/cm²] | Energy [MeV/u] | Range [µm] | Fluence [particles/cm$^2$] |
|---|---|---|---|---|---|---|
| Au | 60 | none | 163 | 15 | 72 | 1x10$^7$ |
| Au | 30 | none | 103.8 | 15 | 71 | 4x10$^7$ |
| Au | 0 | none | 80.2 | 15 | 155 | 2x10$^7$ |

**Table 1: Main characteristics of used heavy ion beam.**

The test setup described in [SWI04-b] was made up with the intention of being able of recovering from any failure condition without needing a power cycle. During the test runs, the DUT core and IO voltages and current consumption were captured and recorded in a running log. Maximum current triggers were set on the power supplies in the event of a latch-up condition that would result in excessive current draw. Due to the high fluxes and total fluences used for the latch-up testing, it was expected that the DUT would lose its programming early in the run and would likely be subject to multiple SEFI conditions during the run. The purpose of the experiment is to demonstrate hardware survivability and soft recovery without the need for a device power cycle.
The Virtex-II XQR2V3000 device showed no latch-up during Au heavy ion irradiation test up to an LET of 160 MeV-cm$^2$/mg and total fluences of 7x10$^7$ particles/cm$^2$.

### 4.1.2 FPGA ARCHITECTURE SUSCEPTIBILITY

Several studies have been performed to analyze Virtex-II susceptibility either to proton and heavy ions. Here we will mention some of them divided by different architectural modules. As said in the previous section we may differ into two well separated groups, the static configuration memory that may not change at all during normal operation, and the dynamic part of the device that are indeed the running modules, logic and Block RAMs inside the FPGA.

#### 4.1.2.1 Static Tests

The test results described here are the radiation test performed by the SEE Consortium created by JPL (NASA) and Xilinx for testing reconfigurable Xilinx FPGAs to evaluate their reliability for space missions. This consortium is formed by several member from US companies, national laboratories and universities (i.e. JPL, Boeing Satellite Systems, LANL, Xilinx, etc.). The test report can be found in depth at [SWI04-c].
For the test setup they have used a prototype board to introduce the three specific Virtex-II radiation tolerant devices, 2V1000, 2V3000 and 2V6000. An external software inside a PC performs readbacks of the configuration memory in order to count the number SEU that impacted on it. This application has also other capabilities as read Block RAMs, internal control registers and reconfigure communication ports if needed.

Both, heavy ions and protons test where performed in order to quantify the impact of these two different particles and correlate them with each specific mission space environment.

##### 4.1.2.1.1 Heavy Ions

HI tests were performed at the Cyclotron Institute, Texas A&M University in June, August, and November 2002 and at Berkeley National Laboratory, UC Berkeley in October 2002.

After applying Edmonds and Weibull parameters to the test results, the saturated cross section of the Virtex-II device is shown in the following table:

| **Parameters** | **Edmonds** | | **Weibull** | | | |
|---|---|---|---|---|---|---|
| **Cells** | **$L_{1/e}$** | **$\sigma_{sat}$ MeV-cm$^2$/mg** | **Limit Cm$^2$** | **Onset MeV-cm$^2$/mg** | **Width -** | **Power -** |
| Configuration bits – TAM (Fig 4) | 5.3 | 3.8E-8 | 4.37E-8 | 1.0 | 33 | 0.8 |
| Configuration bits – LBL (Fig 5) | 2.0 | 3.5E-8 | 4.00E-8 | 1.5 | 7 | 0.3 |
| BRAM - TAM (Fig 6) | 7.0 | 4.7E-8 | 4.19E-8 | 1.0 | 17 | 0.9 |
| BRAM - LBL (Fig 7) | 1.7 | 4.0E-8 | 3.69E-8 | 1.2 | 2 | 0.8 |

**Table 2: Edmonds and Weibull Parameters for Configuration Cells Sensitivities to SEUs.**

Here we may see a graphical approach of the data gathered for configuration bits and block RAMs respectively:

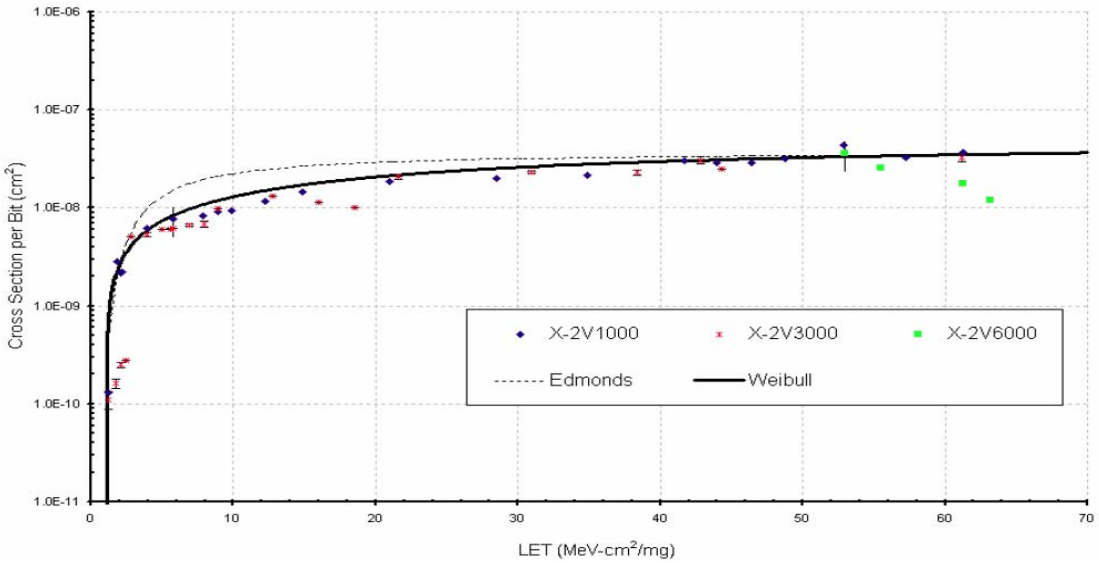


**Figure 9: Virtex-II Configuration Memory Cells Heavy Ions SEU Cross Section.**

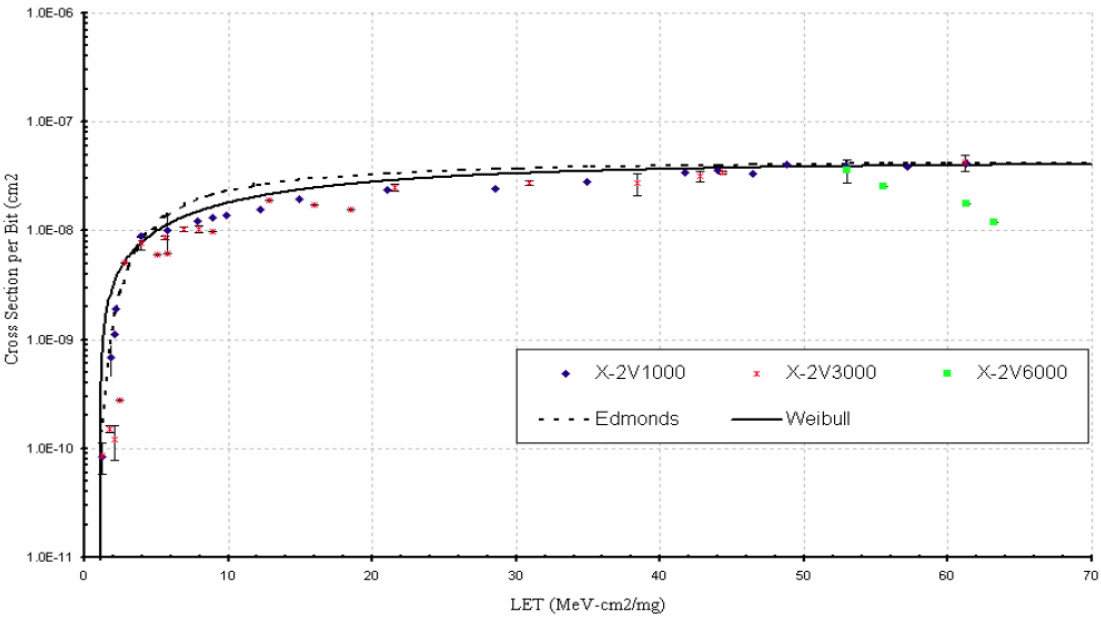


**Figure 10: Virtex-II Block Memory Cells Heavy Ions SEU Cross Section.**

#### 4.1.2.1.2 Protons

Proton radiation testings were performed at IUCF in February 2002, at LBL in January 2003 and at the Crocker Nuclear Laboratory, UC Davis (UCD) in February, April, May and June 2002.

The following table summarizes the device sensitivities to SEUs:

| Energy [MeV] | Facility | Exposed Part Virtex-II- | Fluence [particles/cm$^2$] | CLB Cross Section [cm$^2$] | BRAM Cross Section [cm$^2$] |
|---|---|---|---|---|---|
| 198 | IUCF | 2V1000 | $4.54x10^{13}$ | $3.21x10^{-14}$ | $3.52 x10^{-14}$ |
| 198 | IUCF | 2V6000 | $4.54x10^{13}$ | $2.99x10^{-14}$ | $3.36 x10^{-14}$ |
| 150 | IUCF | 2V1000 | $3.00x10^{11}$ | $3.79x10^{-14}$ | $3.79 x10^{-14}$ |
| 150 | IUCF | 2V6000 | $5.00x10^{11}$ | $3.31 x10^{-14}$ | $3.76 x10^{-14}$ |
| 104 | IUCF | 2V1000 | $6.01x10^{11}$ | $3.75 x10^{-14}$ | $4.09 x10^{-14}$ |
| 104 | IUCF | 2V6000 | $9.41x10^{11}$ | $3.03 x10^{-14}$ | $3.47 x10^{-14}$ |
| 74 | IUCF | 2V1000 | $1.60x10^{12}$ | $3.60 x10^{-14}$ | $3.95 x10^{-14}$ |
| 74 | IUCF | 2V6000 | $1.00x10^{12}$ | $2.83 x10^{-14}$ | $3.21 x10^{-14}$ |
| 40 | LBL | 2V1000 | $1.25x10^{12}$ | $4.20 x10^{-14}$ | $4.76 x10^{-14}$ |
| 20 | LBL | 2V1000 | $4.64x10^{12}$ | $1.75 x10^{-14}$ | $1.96 x10^{-14}$ |
| 14.9 | UCD | 2V1000 | $6.34x10^{12}$ | $3.65 x10^{-14}$ | $3.96 x10^{-14}$ |
| 12 | LBL | 2V1000 | $4.15x10^{12}$ | $6.47 x10^{-15}$ | $6.57 x10^{-15}$ |
| 11.73 | UCD | 2V1000 | $9.01x10^{12}$ | $2.82 x10^{-14}$ | $2.98 x10^{-14}$ |
| 8.8 | UCD | 2V1000 | $2.40x10^{12}$ | $7.22 x10^{-15}$ | $4.74 x10^{-15}$ |
| 8.7 | UCD | 2V6000 | $7.46x10^{12}$ | $7.30 x10^{-15}$ | $5.79 x10^{-15}$ |
| 6.8 | UCD | 2V1000 | $1.73x10^{13}$ | $9.73 x10^{-15}$ | $8.35 x10^{-15}$ |
| 5.3 | UCD | 2V1000 | $1.50x10^{11}$ | $1.40 x10^{-14}$ | $1.25 x10^{-14}$ |
| 3.8 | UCD | 2V1000 | $1.15x10^{12}$ | $9.10 x10^{-15}$ | $7.41 x10^{-15}$ |

**Table 3: Measured cross section under proton beam.**

The following graphs show the saturated cross section vs. proton energy for configuration bits and block RAM respectively:

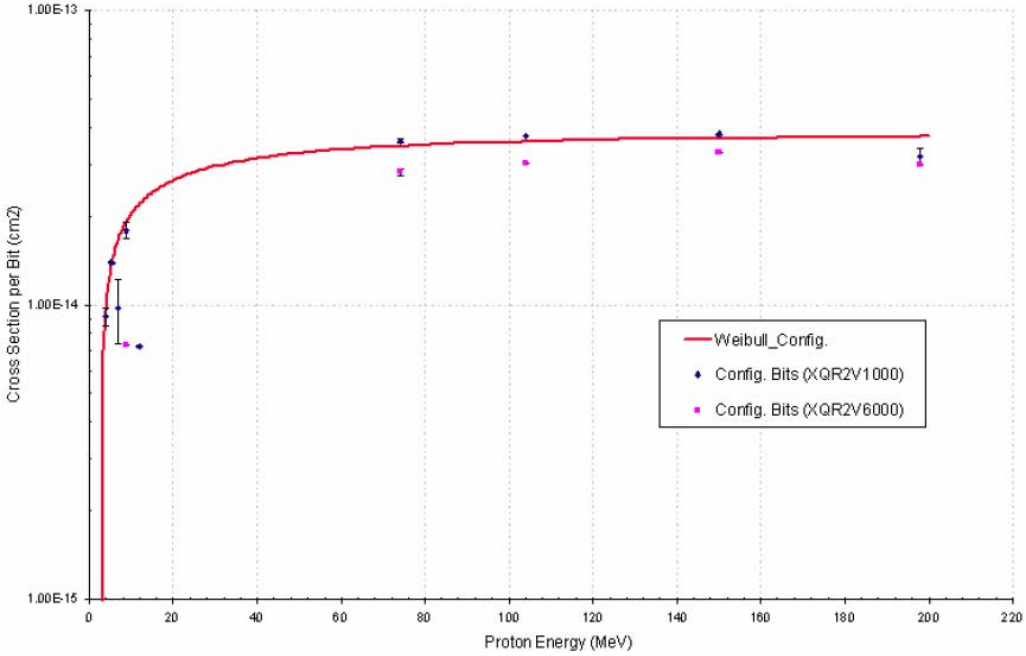


**Figure 11: Virtex-II Configuration Memory Cells Protons SEU Cross Section.**

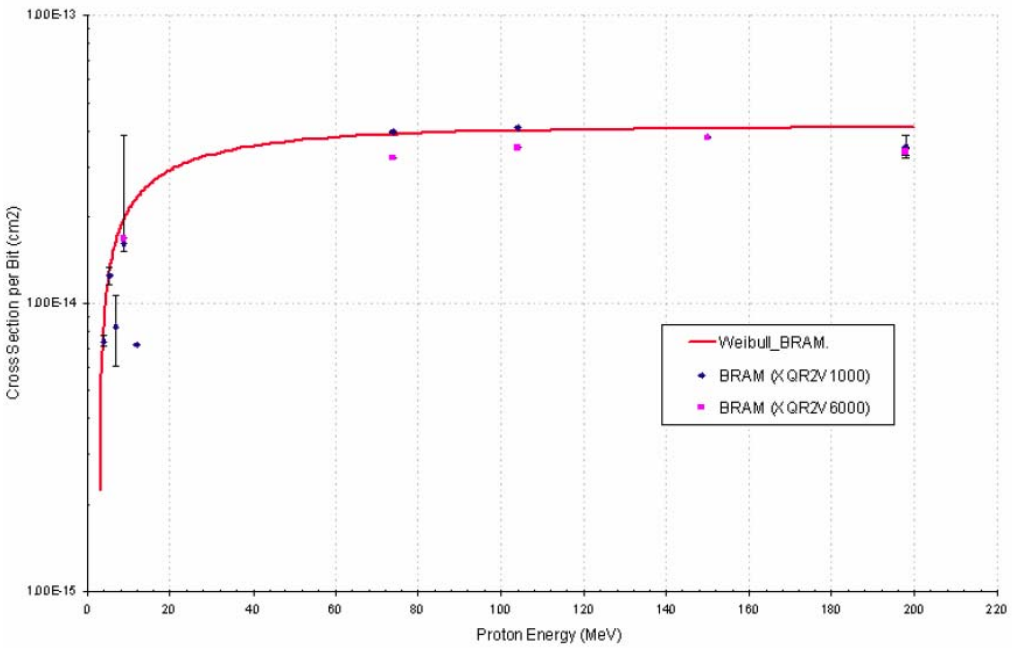


**Figure 12: Virtex-II Block Memory Cells Protons SEU Cross Section.**

#### 4.1.2.2 Dynamic Tests

The dynamics test performed to Virtex-II FPGA on [SWI05-b] are much more complex than the static ones because real time error detection and correction must be applied. Is not the intention of this document to describe deeply the test setup but to inform about the test results gathered on it.

The dynamic tests of the Virtex-II FPGA were focused on two specific functional blocks, the Input/Output Blocks (IOBs) and the Digital Clock Managers (DCMs). The IOBs are the gateways for passing all data on and off the chip while the DCMs synchronize the global clock signals. Testing and analysis of mitigation strategies targeting the functions used in typical designs such as the Configurable Logic Blocks (CLBs), the embedded multipliers, and embedded block RAM are also reported.

##### 4.1.2.2.1 I/O Blocks Test

Three different designs have been tested in order to validate the mitigation techniques.

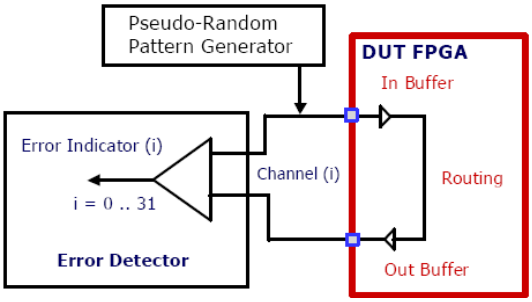


**Figure 13: "No TMR" or "unprotected" control case. It has a single input connected with minimum routing to a single output and uses two external pins.**

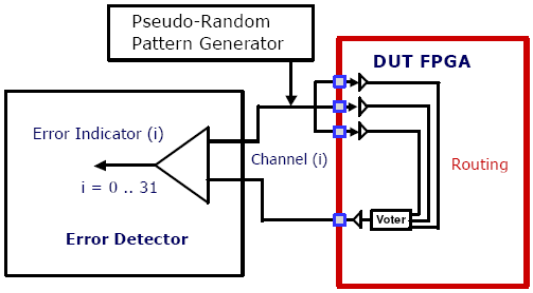


**Figure 14: "TMR-in Only" case and uses three IOBs as triplicated inputs connected to a single IOB for output using minimum routing and a single majority voter. Thus, each channel requires tour pins.**

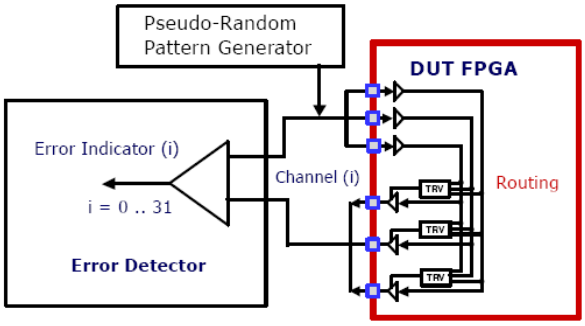


**Figure 15: "Full TMR" case and uses three IOBs as triplicated inputs to three more IOBs configured as triplicated outputs with minimum routing and triplicated minority voters. Each channel requires 6 pins.**

All the tests performed were combined with a 0.5 Hz scrubbing rate. This prevented multiple upset for the same channel to appear.

The result for the sensibility to SEU in the three methods is shown in the following figure. Each color represents ions with different LETs and results are separated by the mitigation technique used.

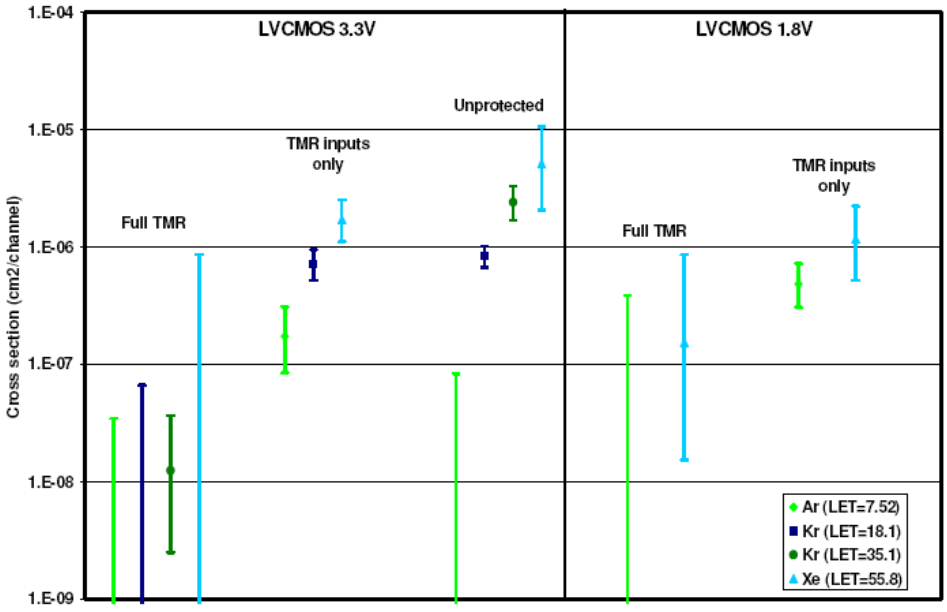


**Figure 16: I/O block test results for LVCMOS using various mitigation techniques.**

For each channel of the NO TMR technique around 238 bits are involved (55 bits each input, 63 bits each output, and an average of 120 bits in the routing). Before going to the radiation

facility, fault injection techniques were used to figure out how many bits were indeed susceptible to provoke an error on the output of a channel. Only 3 bits on the inputs and 8 bits on the outputs were sensitive bits. When XTMR was used (i.e. Full TMR), no sensitive bits were found. This results were indeed ratified with the beam results.

#### 4.1.2.2.2 DCM Test

For testing Digital Clock Managers a test setup with an external monitor was built.

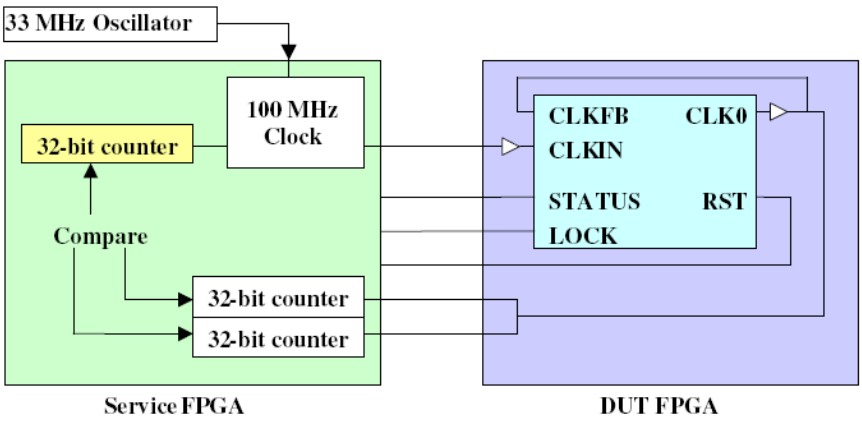


**Figure 17: Block diagram of the test setup for DCM. Duplicated outputs avoids interference of IO Blocks in the measurements.**

Every kind of errors where found while radiating: stack at logic cero or one, extra or missing clock edge, frequency changes and transient errors. Every time an error was detected, the beam was stopped and either a reset, a scrub cycle or both resolved the error. This test was intended to find out the cross section of DCM as well to find the method to recover from DCM failure. Cross section may found to be somewhat the same as for IO Blocks, regarding that 60 bits were responsible for configuring each DCM.

However no mitigation techniques were thought to prevent errors in DCM at the date this test was performed. This means that even though scrubbing would fix the error, up to the scrubbing time a functional error will surely occur because of the clock error. New info recently found from the SEE Consortium, says that they has developed a new mitigation scheme. This method has not been tested yet at any radiation facility though.

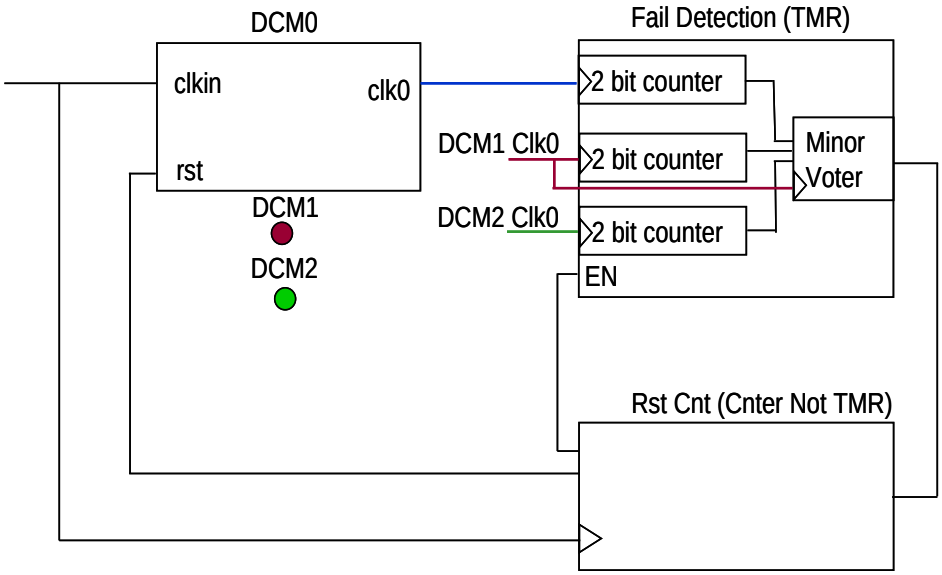


**Figure 18: DCM Mitigation Scheme.**

#### 4.1.2.3 SEFI Phenomenon

The criteria to distinguish a SEFI from a SEU, is that a complete reconfiguration cycle is needed to resolve the error or that is not possible to avoid it with redundancy. There are four types of distinguish SEFI:

1. Power On Reset (POR): a SEU provokes a power on reset of the whole circuit.
2. SelectMAP: SelectMAP port becomes unreadable or with erratic behavior.
3. JTAG: JTAG port becomes unreadable or with erratic behavior.
4. Input/Output Block: it's not possible for a single bit flip to change an input into an output or vice versa, however it may put a whole bank into high impedance state. This SEFI may be corrected with a scrubbing cycle.

Typically, SEFIs are low in occurrence and are quite rare to be seen while in orbit; however it is much easy to find them in test environments due to the high radiation rates and fluxes used to accelerate the process.

The SEFI cross sections for heavy ions and protons are shown in the following tables.

| Heavy Ion | Effective LET [MeV/mg/cm²] | Energy [MeV/u] | Range [µm] | Fluence [particles/cm²] | POR SEFI Cross Section [cm²] | SMAP SEFI Cross Section [cm²] | JCFG SEFI Cross Section [cm²] |
|---|---|---|---|---|---|---|---|
| Xe | 63.3 | 24.8 | 35 | 4.51E+06 | 1.11E-06 | 4.43E-07 | 2.22E-07 |
| Xe | 61.3 | 24.8 | 51 | 2.45E+06 | 8.89E-07 | 4.08E-07 | 1.00E-55 |
| Kr, Xe | 52.9 | 24.8 | (109, 174)* | 2.99E+06 | 3.04E-06 | 1.34E-06 | 1.00E-55 |
| Kr | 50 | 24.8 | 143 | 1.16E+06 | 1.72E-06 | 1.72E-06 | 1.00E-55 |
| Xe | 46.4 | 24.8 | 166 | 4.07E+06 | 2.21E-06 | 1.47E-06 | 1.00E-55 |
| Kr | 41 | 24.8 | 223 | 1.13E+07 | 9.70E-07 | 1.15E-06 | 9.49E-08 |
| Kr, Cu | 29.9 | 40.0 | 117 | 3.98E+06 | 1.26E-06 | 7.54E-07 | 2.51E-07 |
| Kr | 21.0 | 25.0 | 273 | 5.42E+06 | 1.29E-06 | 1.11E-06 | 1.00E-55 |
| Ar | 16.2 | 4.50 | 30 | 3.97E+06 | 2.52E-07 | 1.76E-06 | 1.00E-55 |
| Ar | 12.2 | 40.0 | 73 | 6.42E+06 | 4.67E-07 | 4.67E-07 | 1.00E-55 |
| Ar | 11.7 | 25.00 | 211 | 1.11E+07 | 5.41E-07 | 3.60E-07 | 1.00E-55 |
| Ar | 9.84 | 40.0 | 128 | 4.02E+06 | 1.00E-55 | 2.49E-07 | 1.00E-55 |
| Ar | 8.95 | 40.0 | 163 | 1.20E+07 | 1.67E-07 | 5.00E-07 | 1.00E-55 |
| Ar | 7.89 | 40.0 | 217 | 9.00E+06 | 2.22E-07 | 1.11E-07 | 1.00E-55 |
| Ar, Ne | 7 | 24.8 | 85 | 7.26E+06 | 2.76E-07 | 1.38E-07 | 1.00E-55 |
| Ne | 6.62 | 4.50 | 37 | 2.45E+06 | 4.09E-07 | 4.09E-07 | 1.00E-55 |
| Ne | 5.76 | 25.0 | 457 | $2.84x10^{7}$ | 2.82E-07 | 1.41E-07 | 1.00E-55 |
| Ar | 5.55 | 40.00 | 714 | 1.99E+06 | 1.00E-55 | 1.00E-55 | 1.00E-55 |
| Ne | 4.31 | 40.00 | 228 | 1.20E+07 | 1.00E-55 | 8.33E-08 | 1.00E-55 |
| Ne | 3.7 | 40.0 | 1016 | 2.31E+07 | 1.00E-55 | 8.65E-08 | 1.00E-55 |
| Ne | 3 | 40.00 | 396 | 1.68E+07 | 1.19E-07 | 1.78E-07 | 1.00E-55 |
| Ne | 2.4 | 40.00 | 520 | 8.12E+07 | 1.23E-08 | 3.70E-08 | 1.00E-55 |
| Ne | 2.15 | 40.0 | 455 | 1.70E+07 | 1.00E-55 | 1.00E-55 | 1.00E-55 |
| Ne, B | 1.80 | 24.8 | (1122, 735, 63)* | 2.99E+08 | 1.00E-08 | 1.00E-08 | 1.00E-55 |
| Ne | 1.21 | 40.0 | 1593 | 3.55E+07 | 1.00E-55 | 1.00E-55 | 1.00E-55 |

**Table 4: SEFI cross section for Heavy Ions.**

| Energy [MeV] | Facility | Exposed Part Virtex-II- | Fluence [particles/cm²] | POR SEFI Cross Section [cm²] | SMAP SEFI Cross Section [cm²] | JCFG SEFI Cross Section [cm²] |
|---|---|---|---|---|---|---|
| 198 | IUCF | 2V1000 | $4.40x10^{13}$ | $3.6x10^{-13}$ | $5.5x10^{-13}$ | $2.7x10^{-13}$ |
| 150 | IUCF | 2V1000 | $8.00x10^{11}$ | * | $1.3x10^{-12}$ | * |
| 104 | IUCF | 2V1000 | $1.54x10^{12}$ | * | $6.5x10^{-13}$ | $6.5x10^{-13}$ |
| 74 | IUCF | 2V1000 | $2.60x10^{12}$ | * | $7.7x10^{-13}$ | $3.8x10^{-13}$ |
| 40 | LBL | 2V1000 | $1.25x10^{12}$ | $8.0x10^{-13}$ | $1.6x10^{-12}$ | $8.0x10^{-13}$ |
| 20 | LBL | 2V1000 | $4.64x10^{12}$ | $2.2x10^{-13}$ | * | * |
| 14.9 | UCD | 2V1000 | $6.34x10^{12}$ | $3.1x10^{-13}$ | * | * |
| 11.73 | UCD | 2V1000 | $1.27x10^{13}$ | $7.9x10^{-14}$ | $3.9x10^{-13}$ | $1.6x10^{-13}$ |
| 8.8 | UCD | 2V1000 | $9.86x10^{12}$ | $2.0x10^{-13}$ | $3.0410^{-13}$ | $1.0x10^{-13}$ |
| 6.8 | UCD | 2V1000 | $1.73x10^{13}$ | * | $1.2x10^{-13}$ | $5.8x10^{-14}$ |
| 3.8 | UCD | 2V1000 | $1.15x10^{12}$ | * | * | * |

* none observed for the given fluence

**Table 5: SEFI cross section for Protons.**

As shown in the tables above, the probability of SEFIs induced by protons is almost cero, while induced by HI is quite rare too. However this errors are not avoiding errors and the must be taken into accounts when using single device systems.

## 4.2 CR-II TEST

The aim of this irradiation campaign was to evaluate the behavioral of the Xilinx® CoolRunner-II™ CPLD technology in harnessing radiation environment. This technology provides ultra-low power consumption while keeps a really good relationship between area

and logic capacity. All these qualities make this technology very suitable for satellites with low power budget and area constraints.

There were three main goals to achieve during the qualification campaign:

1. Determine the technology susceptibility to single event latch-up. If the technology is latch-up susceptible to proton energies bellow 60 MeV, it will be useless for space missions.
2. Determine the configuration Flash memory susceptibility to SEU. This Flash memory keeps the configuration of the device during the whole mission, and from it the configuration is downloaded to the SRAM-based running logic. If this memory is susceptible to change during mission, no possible recovery may be performed. Thus, the device will become useless at some early point during mission.
3. Determine the grade of susceptibility of the RAM-based logic to SEU. Even though it is foreseen that the RAM part will be susceptible to protons hits, it is important to quantify its susceptibility in order to evaluate the reliability of the device.

There is a fourth issue that will be inherently measure. When testing with low energy protons, TID on each part will rise to values upper 20 Krad. A power consumption setup has been also built up in the Control Board in order to monitor if it is increasing due to Total Ionizing Dose. Although, an alpha particles test has been foreseen after the proton irradiation campaign to determine the TID immunity of this technology. The results of this test will also be reported.

### 4.2.1 IRRADIATION FACILITY

Proton testing was conducted in Paul Scherrer Institute (PSI) at the Proton Irradiation Facility (PIF) components in the low energy area (NEB).

Examples of the energy spectra for protons with energies of 64 MeV and 23 MeV are shown in Figure 19. The measurements were done using plastics scintillator NE102 of 35 mm thickness to stop the protons. No corrections due to a finite resolution and scattering effects are made. Beam profiles are usually set to flat during the setup using small Copper plate located in the beam-line about 2 m upstream. One assures the uniform field of up to 5 cm diameter at each energy channel. For smaller beam diameters the Copper plate must be removed. Without the plate can achieve beam diameters as small as 0.5 cm.

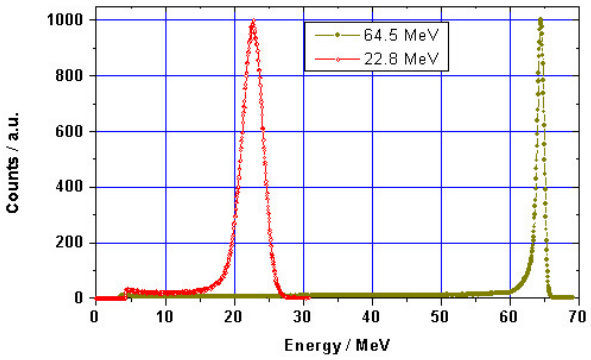


**Figure 19. PIF-NEB Examples of energy spectra.**

Energy beams available in the low energy NEB facility are presented in the Table 6:

| Low energy proton beams | |
|---|---|
| **Energy (MeV)** | **LET (MeV/mg/cm2)** |
| 10,76 | 3,270E-02 |
| 14,59 | 2,584E-02 |
| 20,53 | 1,979E-02 |
| 25,34 | 1,678E-02 |
| 30,29 | 1,458E-02 |
| 39,92 | 1,174E-02 |
| 49,85 | 9,879E-03 |
| 62,91 | 8,259E-03 |

**Table 6. NEB low energy proton beams. Values update to 13/02/2007.**

Main features of the irradiation facility are:

- **Energy range:** The energy can be selected in a semi-continuous manner between 6 and 63 MeV by placing a proper material thickness on the beam axis. See Table 6.
- **Proton flux**: < $5x10^8$ p/$cm^2$/sec.
- **Beam spot**: circle, up to 9 cm diameter.
- **Beam uniformity**: > 90% over 5 cm diameter.
- **Flux/Dissymmetry**: about 5% absolute accuracy.
- Irradiation takes place in air.

### 4.2.2 DEVICE INFORMATION

Only relative information to proton test will be notice in this section. Further descriptions about CR-II CPLDs may be found [CR208] and [CR202].

The DUT has three important sensibilities areas that has been monitored and tested.

1. Non-volatile Configuration Memory: as its own name indicates, this memory keeps data even when no voltage is applied to CR-II. The function of this memory is to keep the configuration bit stream unchangeable. Whenever the device is powered up, this bit stream is transferred to volatile configuration memory.
2. Volatile SRAM Configuration Memory: this memory actually configures the device and describes its behavior. However every time the device is powered down SRAM cells are deleted.
3. Combinational Logic: although this logic is SEU sensitive too, its low density compare with configuration memory makes probability decrease extremely when talking about SEFIs induced by combinational logic.

### 4.2.3 DUT CHARACTERISTICS

DUT specific characteristics are shown in the following Table 7:

| **Part Number** | **XC2X512-7PQG208C** |
|---|---|
| Category | CPLD (Complex Programmable Logic Device) |
| Manufacturer | Xilinx Inc. |
| Family | CPLD / EEPLD |
| Technology | CMOS |

| | |
|---|---|
| Number of Samples | 6 (2 for backup) |
| In-system Program | YES |
| JTAG BST | YES |
| RoHS Compliant | YES |
| Package Style | PQFP208, HQG208 |
| Package Equivalence Code | PQG208 |
| Package Material | PLASTIC |
| Number of PINS | Total = 208 / User = 173 |
| Mountain Style | Surface Mount (SMD) |
| Reliability Level | Commercial |
| Min Operational Temp. | 0 ºC |
| Max Operational Temp. | +70 ºC |
| Power Supply | CORE: 1.8V<br>I/O: 3.3V<br>JTAG: 3.3V |
| Max Supply Current (mA) | 1 mA at 1Mhz in dynamic mode |
| Number of Configuration bits | 296403 |
| Number of Macrocells | 512 |

**Table 7: XC2C512-7PQG208C Characteristics**

### 4.2.4 TEST PROCEDURE

This section will be divided into three different subsections. First one (Test Setup) will describe completely the hardware configuration and its functionality. The second one (Test Plan), will show every step we took in the test and what kind of tests did we perform. Finally the third part describes the personnel in charge of the different duties.

#### 4.2.4.1 TEST SETUP

The following figure shows the five important subsystems (labeled in blue) developed for all different tests performed to CoolRunner-II CPLDs. Afterwards all subsystems will be separately described:

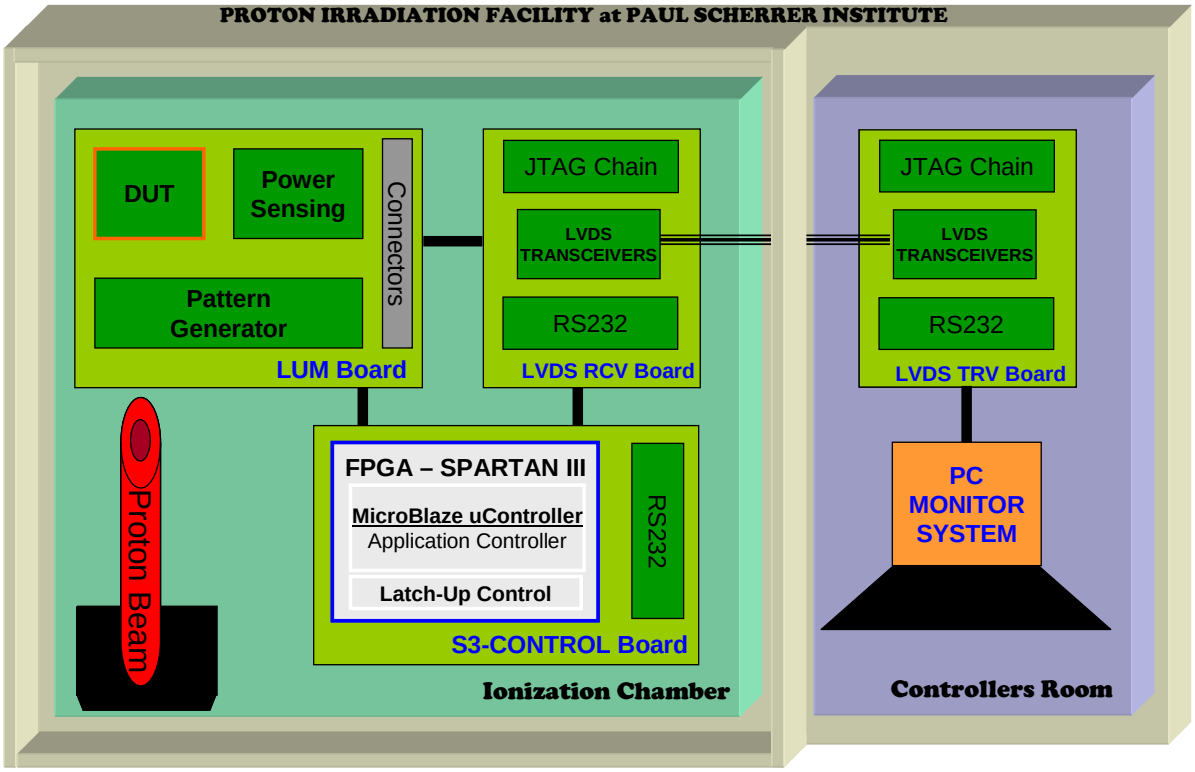


**Figure 20: Test Setup inside Proton Irradiation Facility (PIF) at Paul Scherrer Institute.**

As shown in figure, signals between Controller's Room and Ionization Chamber are sent through LVDS channels to ensure signal integrity between the 30m distance. A PC Monitor System is used at Controller's Room to check real time information and perform some other actions explained below on section 4.2.5.
A FPGA based board (S3-Control board) is situated 2 meters apart from DUT. This board will interface between LUM Board and PC Monitor, and also perform real time hardware check of DUT application. Further explanations of these components are written below.

#### 4.2.4.1.1 LATCH-UP MOTHERBOARD (LUM)

LUM Board contains the Device under Test and therefore is the one situated in front of the proton beam. DUT is actually soldered on a skirting board that may be easily inserted and extracted from the LUM Board. Thus we could change between several parts avoiding TID to interfere in the measurements.
For the dynamic tests (explained on section 4.2.5.2) a pattern generator has been included in the LUM Board. This pattern generator receives commands from S3-Control Board to start and stop running. It has been implemented in a smaller CoolRunner-II situated in the opposite corner from the DUT. Pattern used was two operands that will act as inputs of the mathematical operations performed by the DUT. Finally, results will be sent towards S3-Control Board to check them.

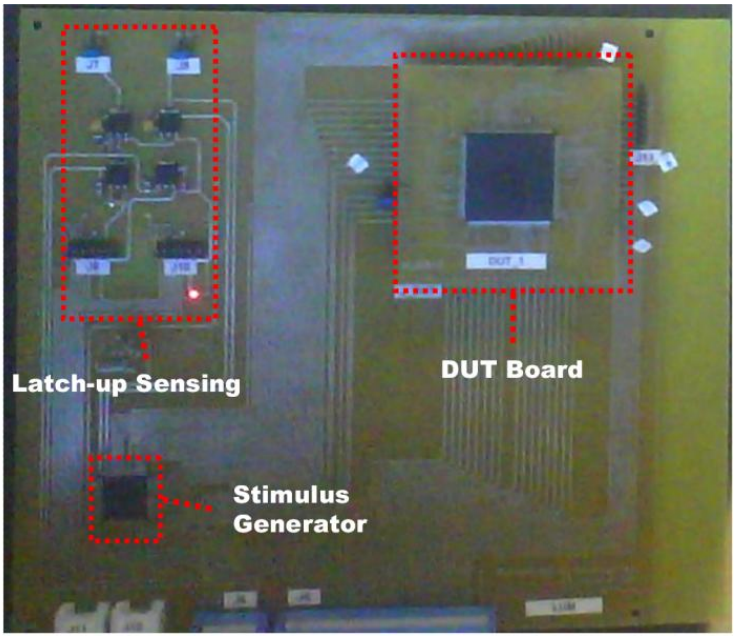


**Figure 21: Latch-Up Motherboard (LUM) description.**

#### 4.2.4.1.2 S3-CONTROL BOARD

This is an evaluation board from AvNet with a Spartan-III FPGA commanded by a MicroBlaze micro-processor. The functionality performed by the S3-Control Board will later be explained on section 4.2.5. A 50 pin connector is used for communications between LUM Board and also between LVDS RCV Board. Also JTAG interface is used to close the complete JTAG chain made up by 4 devices:

1. Flash Configuration EEPROM: used to store Spartan's configuration bit stream.
2. Spartan-III FPGA.
3. CoolRunner-II 128: this is the stimulus generator of the DUT application.
4. CoolRunner-II 512: this is the DUT.

The following figure shows the used parts of this board:

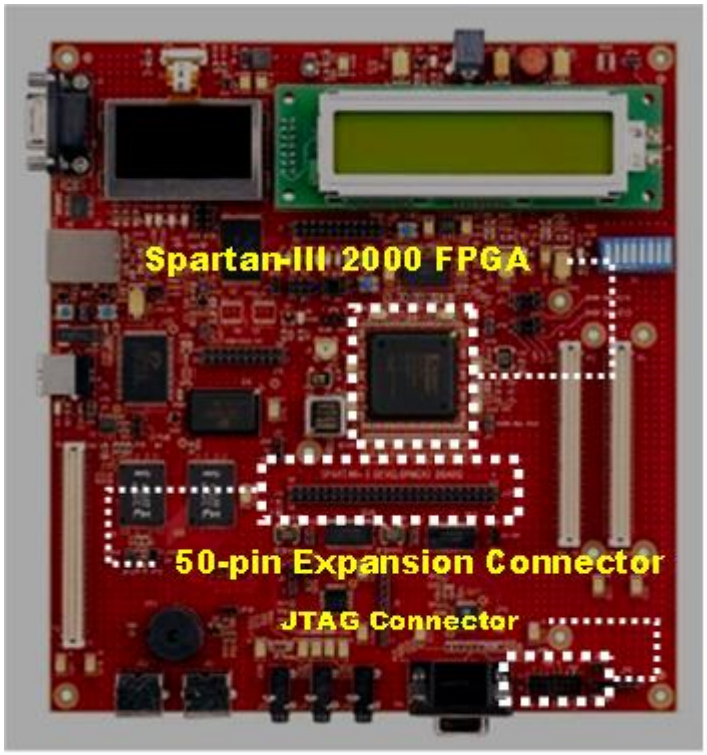


**Figure 22: S3-Control Board.**

#### 4.2.4.1.3 LVDS RCV BOARD

The functionality of this board is only to send and receive signal through LVDS. This is to avoid signal corruption because of the long distance between the Ionization Chamber and the Controllers Room. Thus, this board is equipped with two LVDS transceivers, one for incoming data and one for outgoing data. The data is sent through a 4-pairs differential cable (Ethernet type) and is received in the board through a RJ45 connector. Then signal are distributed towards S3-Control Board and LUM Board.

#### 4.2.4.1.4 LVDS TRV BOARD

The functionality of this board is only to send and receive signal through LVDS. This is to avoid signal corruption because of the long distance between the Ionization Chamber and the Controllers Room. Thus, this board is equipped with two LVDS transceivers, one for incoming data and one for outgoing data. The data is sent through a 4-pairs differential cable (Ethernet type) and is received in the board through a RJ45 connector. JTAG chain is connected to Xilinx Programming Cable and Serial Communications are connected with PC Monitor.

#### 4.2.4.1.5 PC MONITOR SYSTEM

A common laptop has been used. Apart from serial terminal for monitoring duties, another application has been used for static test explained on section 4.2.5.1.

### 4.2.5 TEST PLAN

In order to be able to understand the radiation test performed to CR-II CPLD we must first describe how these devices work, and what parts do they have to be tested.

CR-II has two separated configuration memories. The first one is a non-volatile Flash type memory. This memory is used to store the configuration of the CPLD during power down mode. The second configuration memory is a SRAM based memory; therefore configuration bit stream is not keep during power down mode. There are several reasons of why CR-II uses these two configuration memories (access time, power consumption, on the fly configuration, etc) however this is not the point of this thesis and we will not explain them. The point is that Flash memory is in charged of storing the bit stream; however it is parallel copied to the SRAM memory that is the one that actually configures the logic inside the CPLD.
CR-II is also made up logic cells, registers and IO Blocks. We will clearly separate these other parts in a separate group because of two reasons:

1. This logic is not readable directly and is not distributed by the manufacturer.
2. The size of this logic is about the 10% of the size of the configuration memories.

Configuration memories may be read from our PC Monitor with a developed dedicated tool created specifically for this test. Therefore testing SEUs in configuration memory is quite easy. However when attempting to check SEU effects on the CPLD logic, is not possible read a map of this logic, therefore we only may check the correct functionality of the application running on it. Because of this, we have separated test on two different sections. First section or static test will check SEU susceptibility on both configuration memories. Dynamic test are set to find the MTBFF of the application running inside the CR-II CPLD.

#### 4.2.5.1 STATIC TEST

PC Monitor System is the one in charged of performing periodical memory check of the DUT while been under radiation. The tool created for this duty is a Tcl application that interacts with Xilinx Programming Tool (Impact) in order to read the bitstreams from both memories. This tool is capable of reading SRAM memory every 3 seconds and Flash memory every 5 seconds. We have programmed the tool to perform five SRAM readbacks per each Flash readback. We have chosen this 5 to 1 proportion because we expected that Flash memory is much less sensitive to protons than SRAM memory.
Our principal aware on these tests is to see how sensitive Flash configuration memory is. This is because SRAM memory can be reconfigured by a power cycle, however to reconfigure the non-volatile memory a specific circuit bigger even than the CPLD must be used. Thus, SEUs in the SRAM memory are much more easily managed than over Flash memory. Also we where quite concern about how could SEUs affect Flash memory while powered off. We had then planned some radiation tests over the CR-II device powered off as described later on in this section.
After every memory readback a parallel program performs a comparison between the two last bit streams and stores the number of SEUs (changes from “cero to one” and from “one to cero”), and then displays them in real time. Next figure shows a line time diagram of the readback tool:

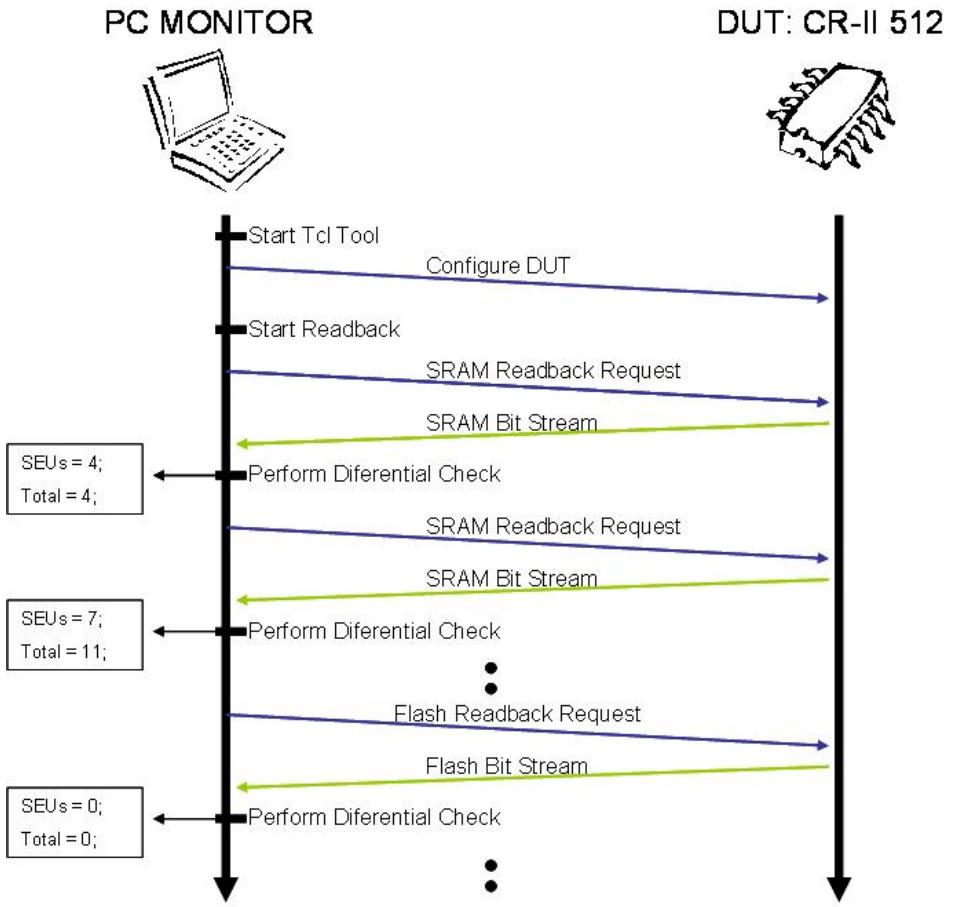


**Figure 23: Tcl Readback Tool.**

In order to get an accurate cross section of the device, we will collect data until 100 SEUs occurred. However, we do not foresee too much SEUs at low energies, and therefore we will radiate DUT up to 1e10 p+/cm2 or until 100 SEUs are detected at each energy step. These are the Static test we have planned:

- Test 1: Seven runs will be performed from 60 MeV down to 10 MeV p+. At each energy step the run will finish when 100 SEUs had occurred or when fluency has reached 1e10 p+/cm2. The DUT will be configured with a concrete pattern bit stream.
- Test 2: same as Test 1 with a new device.
- Test 3: A unique run with a different device and with 60 MeV energy will be performed. However this time we will radiate the DUT up to 1e11 p+/cm2. We want to see how Flash memory behaviors with very high fluencies.
- Test 4: Two runs with a new device will be performed. However this time the device will be powered down during radiation. Firstly we will configure the device, and then we will cut power and start radiating up to 1e10 p+/cm2. When max fluency has been reached, we will perform a readback to check SEUs on Flash memory. The second run will be the same but reaching 9e10 p+/cm2 fluency._These test are meant to check Flash susceptibility when not powered.

#### 4.2.5.2 DYNAMIC TEST

The application to be run inside the DUT is a segmented multiplier with two 10-bits operands and 20-bit result. The operands will be generated by the Stimulus Generator device (also a

CR-II CPLD) that will be commanded by the FPGA in the S3-Control Board. The following figure shows the interface block diagram:

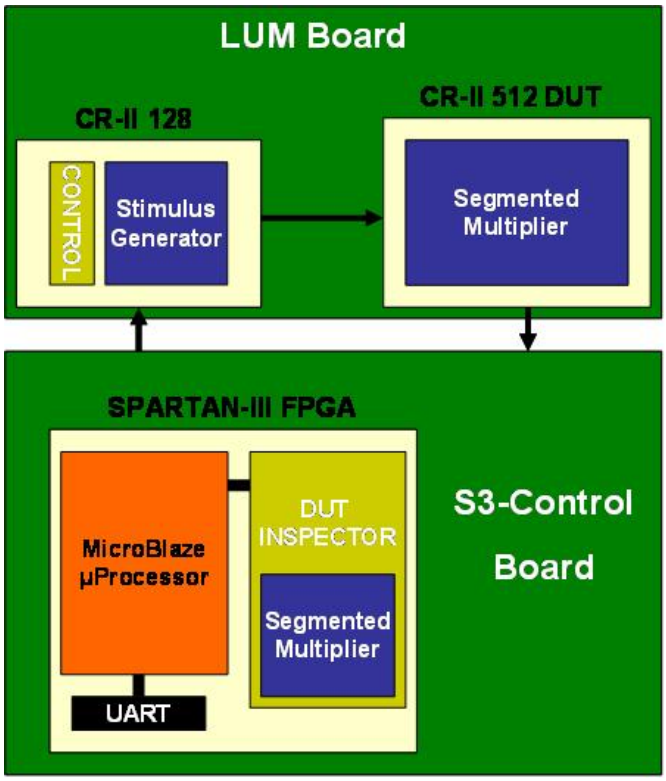


**Figure 24: Dynamic Test Block Diagram.**

As seen in figure above there are three main contributors of the running application. Also the user will interact with the processor through the UART to start/stop the application and to receive real time data of the test status.
The process was run as follows:

1. The user sends the Start command to the S3-Control Board.
2. The FPGA generates the Start signal towards Stimulus Generator on LUM Board.
3. With a 1 MHz clock, the CR-II 128 starts sending operand 'A' and operand 'B' towards DUT.
4. Each cycle (1 us) a new result is resolved by the CR-II under test and sent to the FPGA.
5. The FPGA checks the given result and in case of error generates an error interrupt to inform the user about it.
6. If an error was signaled, a power cycle will reconfigure the DUT to continue the test straight forward. Even though it would be better to not configure the device while being irradiated, due to facility operative tools, it was very difficult to measure the real irradiation towards DUT, if we would had to stop the beam at each functional error.

The duties of each actor during the dynamic test are described here:

#### 4.2.5.2.1 Spartan-III FPGA

The program running over MicroBlaze uProcessor prompts with a user menu that lets the user to start/stop application (multiplier) and some other info instructions. When user presses start button the processor sends a start command to the Stimulus generator and activates its own inspector system. The inspector starts then to perform the same multiplication that the DUT

must perform in this cycle and then waits for the DUT to send a valid data signal. Multiplier inside FPGA is about 40 times faster; therefore FPGA inspector will not have any problem to check DUT results with the correct ones. Every time DUT sends a valid data signal, the results are compared. If a mismatch occurs an internal counter is incremented and the error is signaled to the user. As will be explained later, an error on the result may be caused either by a SEU on the logic, or by a SEU on the configuration memory. If the memory was the cause, then following results will be affected too. In this case the processor powers down and up the DUT in order to reconfigure it and recover from the SEU. The application may be stopped and started at any time.

#### 4.2.5.2.2 CR-II 128 S.G.

The Stimulus Generator has a very simple duty. When receives order from the processor to start generating patterns, it signals the DUT to start multiplying and starts up two counters that will generate up to $2^{20}$ different multiplications. When finishes, the done signal is sent to the DUT and both stop running. The 1 MHz clock used to synchronize both devices makes the whole run to last for something less than one second. When the processor receives the done signal automatically starts the whole process again.

#### 4.2.5.2.3 CR-II 512 DUT

The segmented multiplier has been chosen as the application to be tested because is capable to use almost all the resources available inside the CR-II device. This will help us in order to get a worst case application to be implemented inside these devices. The application starts as soon as receives the start signal from S.G. and starts a new multiplication every cycle (1 MHz). The multiplier is a 5-stage pipeline so results start outgoing towards the FPGA 5 cycles after start signal is asserted and a valid data is signaled every cycle.

For the dynamic test we have also prepared a hardened version of the multiplier. We applied TMR techniques to the multiplier to mask SEUs in the combinatorial logic. We did not plan this to make great differences because two reasons:

1. The logic hardened is only about a 10% of the configuration memory (that may not be hardened in any way). And also,
2. Multiple Event Upsets are not masked.

However TMR could help us in a real application to mitigate first errors and afterwards reconfigure the CR-II with the internal Flash contents, recovering the correct configuration data.

### 4.2.6 TEST REPORT

Six CPLDs have been tested, named DUT1, DUT2, DUT3, DUT4, DUT5 and DUT7. Four of them (DUT1, DUT7, DUT2, DUT3) in static mode to characterize SEU susceptibility. DUT1 and DUT 7 were irradiated powered on in order to test RAM memory. DUT2 and DUT3 powered on and off respectively to test Flash memory in different conditions. Run number in following tables is a consecutive number which starts when first CPLD test starts. Some run numbers are not displayed because they were used to adjust the beam. Partial Dose for each run and total dose at the end of irradiation device is also showed.

#### 4.2.6.1 STATIC TEST

Although "Maximum Fluence" was programmed at $1E^{10}$ protons for each available proton energy, run was stopped when 100 upsets were registered in order to get 10% error in measurement.

The aim of the test in DUT1 and DUT7 was measuring SEU in RAM configuration memory. SEU in Flash was register too but no SEU in Flash memory was detected at these fluencies.

| Static Test Coolrunner Power on CPLD-DUT1 | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| RUN | Energy (MeV) | LET (MeV/mg/cm²) | Flux (p/cm²/s) | Fluence (p/cm²) | Maximum Fluence (p/cm²) | TID (krad) | SEU (SRAM) (Conf. Mem.) | Cross Section per device (SRAM) (Conf. Mem.) | Cross Section per bit (SRAM) (Conf. Mem.) |
| 2 | 62,91 | 8,259E-03 | 1,00E+07 | 5,17E+09 | 1,00E+10 | 0,68 | 100 | 1,93E-08 | 1,93E-12 |
| 4 | 49,85 | 9,879E-03 | 5,87E+07 | 5,18E+09 | 1,00E+10 | 0,82 | 106 | 2,05E-08 | 2,05E-12 |
| 5 | 39,92 | 1,174E-02 | 4,24E+07 | 4,96E+09 | 1,00E+10 | 0,93 | 100 | 2,02E-08 | 2,02E-12 |
| 6 | 30,29 | 1,458E-02 | 3,09E+07 | 5,16E+09 | 1,00E+10 | 1,20 | 101 | 1,96E-08 | 1,96E-12 |
| 7 | 25,34 | 1,678E-02 | 2,03E+07 | 5,69E+09 | 1,00E+10 | 1,53 | 102 | 1,79E-08 | 1,79E-12 |
| 9 | 20,53 | 1,979E-02 | 4,12E+07 | 7,95E+09 | 1,00E+10 | 2,52 | 100 | 1,26E-08 | 1,26E-12 |
| 6 | 14,59 | 2,584E-02 | 3,51E+07 | 1,00E+10 | 1,00E+10 | 4,13 | 31 | 3,10E-09 | 3,10E-13 |
| 15 | 10,76 | 3,270E-02 | 7,01E+07 | 1,01E+10 | 1,00E+10 | 5,28 | 5 | 4,95E-10 | 4,95E-14 |
| | | | | Accumulated TID | | 17,10 | | | |

**Table 8: Static Test Coolrunner Power on CPLD-DUT1.**

| Static Test Coolrunner Power on CPLD-DUT7 | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| RUN | Energy (MeV) | LET (MeV/mg/cm²) | Flux (p/cm²/s) | Fluence (p/cm²) | Maximum Fluence (p/cm²) | TID (krad) | SEU (SRAM) (Conf. Mem.) | Cross Section per device (SRAM) (Conf. Mem.) | Cross Section per bit (SRAM) (Conf. Mem.) |
| 17 | 62,91 | 8,259E-03 | 3,32E+08 | 6,30E+09 | 1,00E+10 | 0,83 | 123 | 1,95E-08 | 1,95E-12 |
| 18 | 39,92 | 1,174E-02 | 1,92E+08 | 5,96E+09 | 1,00E+10 | 1,12 | 112 | 1,88E-08 | 1,88E-12 |
| 19 | 30,29 | 1,458E-02 | 1,50E+08 | 5,40E+09 | 1,00E+10 | 1,26 | 113 | 2,09E-08 | 2,09E-12 |
| 20 | 25,34 | 1,678E-02 | 1,20E+08 | 5,06E+09 | 1,00E+10 | 1,36 | 113 | 2,23E-08 | 2,23E-12 |
| 21 | 20,53 | 1,979E-02 | 1,12E+08 | 6,69E+09 | 1,00E+10 | 2,12 | 100 | 1,49E-08 | 1,49E-12 |
| 22 | 14,59 | 2,584E-02 | 8,61E+07 | 1,01E+10 | 1,00E+10 | 4,18 | 28 | 2,77E-09 | 2,77E-13 |
| 23 | 10,76 | 3,270E-02 | 7,13E+07 | 1,01E+10 | 1,00E+10 | 5,28 | 3 | 2,97E-10 | 2,97E-14 |
| | | | | Accumulated TID | | 16,15 | | | |

**Table 9: Static Test Coolrunner Power on CPLD-DUT7.**

In order to check Flash susceptibility the fluencies in DUT2 (powered off) was increased until $1E^{10}$ (run 24) and $9E^{10}$ (run25) both at 62,91 MeV.
As no SEU was registered in DUT2 when it was powered off, an additional run was made on the device just to confirm the SEU data for RAM (DUT1 and DUT7) at 25MeV

| Static Test Coolrunner DUT2 |
|---|

| RUN | Energy (MeV) | LET (MeV/mg/cm$^2$) | Flux (p/cm$^2$/s) | Fluence (p/cm$^2$) | Time (s) | Maximum Fluence (p/cm$^2$) | TID (krad) | SEU (SRAM) (Conf. Mem.) | SEU (FLASH) (Conf. Mem.) | Cross Section per device (SRAM) (Conf. Mem.) | Cross Section per bit (SRAM) (Conf. Mem.) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **24** | 62,91 | 8,259E-03 | 3,58E+08 | 1,04E+10 | 29 | 1,00E+10 | 1,37 | | **0** | | |
| **25** | 62,91 | 8,259E-03 | 3,66E+08 | 9,04E+10 | 247 | 9,00E+10 | 11,95 | | **0** | | **0,00E+00** |
| **26** | 25,34 | 1,678E-02 | 1,16E+08 | 4,74E+09 | 41 | 1,00E+10 | 1,27 | **107** | | **2,26E-08** | **2,26E-12** |
| | | | | | **Accumulated TID** | | | | **14,59** | | |

**Table 10: Static Test Coolrunner DUT2.**

| Static Test Coolrunner Power on CPLD-DUT3 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RUN | Energy (MeV) | LET (MeV/mg/cm$^2$) | Flux (p/cm$^2$/s) | Fluence (p/cm$^2$) | Time (min) | Maximum Fluence (p/cm$^2$) | TID (krad) | SEU (SRAM) (Conf. Mem.) | SEU (FLASH) (Conf. Mem.) | Cross Section per device (SRAM) (Conf. Mem.) | Cross Section per bit (SRAM) (Conf. Mem.) |
| **27** | 62,91 | 8,259E-03 | 3,71E+08 | 1,00E+11 | 4,5 | 1,00E+11 | 13,21 | **2341** | **0** | **2,34E-08** | **2,34E-12** |

**Table 11: Static Test Coolrunner Power on CPLD-DUT3.**

No SEU was detected Flash Memory in static test with CPLD power on or off.

The following graph shows the obtained cross section of the configuration memory (RAM) in CR-II:

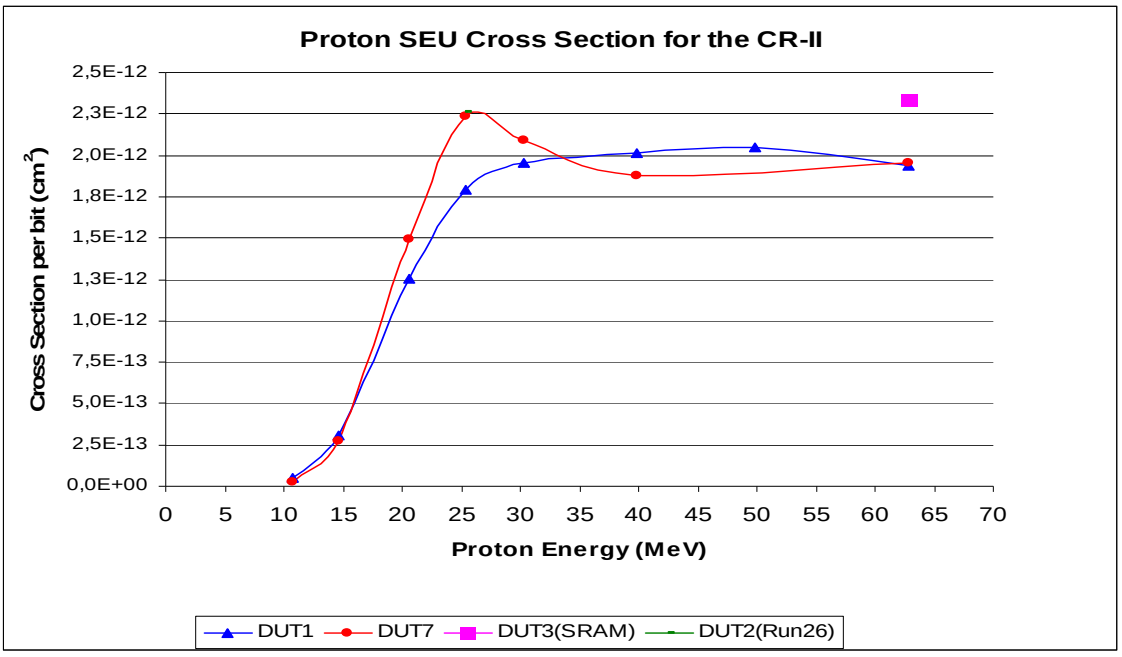


**Figure 25: Proton SEU Cross Section of configuration memory (RAM) for the CR-II.**

### 4.2.6.2 DYNAMIC TEST

| Dynamic Test Coolrunner CPLD-DUT4 |
|---|

| RUN | Energy (MeV) | LET (MeV/mg/cm$^2$) | Flux (p/cm$^2$/s) | Fluence (p/cm$^2$) | Time (min) | Maximum Fluence (p/cm$^2$) | TID (krad) | Errors | Cross Section per device | Cross Section per bit |
|---|---|---|---|---|---|---|---|---|---|---|
| 29 | 62,91 | 8,259E-03 | 7,00E+07 | 1,00E+10 | 2,4 | 1,00E+10 | 1,32 | 57 | 5,70E-09 | 5,70E-13 |
| 30 | 49,85 | 9,879E-03 | 5,59E+07 | 1,00E+10 | 3,0 | 1,00E+10 | 1,58 | 47 | 4,70E-09 | 4,70E-13 |
| 31 | 39,92 | 1,174E-02 | 4,14E+07 | 1,01E+10 | 4,1 | 1,00E+10 | 1,90 | 50 | 4,95E-09 | 4,95E-13 |
| 32 | 30,29 | 1,458E-02 | 3,12E+07 | 1,00E+10 | 5,4 | 1,00E+10 | 2,33 | 46 | 4,60E-09 | 4,60E-13 |
| 33 | 25,34 | 1,678E-02 | 2,56E+07 | 1,00E+10 | 6,6 | 1,00E+10 | 2,68 | 49 | 4,90E-09 | 4,90E-13 |
| 34 | 20,53 | 1,979E-02 | 2,29E+07 | 1,00E+10 | 7,3 | 1,00E+10 | 3,17 | 43 | 4,30E-09 | 4,30E-13 |
| 35 | 14,59 | 2,584E-02 | 1,74E+07 | 1,00E+10 | 9,6 | 1,00E+10 | 4,13 | 10 | 1,00E-09 | 1,00E-13 |
| 36 | 10,76 | 3,270E-02 | 1,40E+07 | 1,00E+10 | 12,0 | 1,00E+10 | 5,23 | **7** | 7,00E-10 | 7,00E-14 |
| | | | | | **Accumulated TID** | | **22,3** | | | |

**Table 12: Dynamic Test Coolrunner CPLD-DUT4.**

| Dynamic Test Coolrunner CPLD-DUT5 | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| RUN | Energy (MeV) | LET (MeV/mg/cm$^2$) | Flux (p/cm$^2$/s) | Fluence (p/cm$^2$) | Time (min) | Maximum Fluence (p/cm$^2$) | TID (krad) | Errors | Cross Section per device | Cross Section per bit |
| 38 | 62,91 | 8,259E-03 | 5,88E+07 | 1,00E+10 | 2,9 | 1,00E+10 | 1,32 | 50 | 5,00E-09 | 5,00E-13 |
| 39 | 49,85 | 9,879E-03 | 4,97E+07 | 1,00E+10 | 3,4 | 1,00E+10 | 1,58 | 66 | 6,60E-09 | 6,60E-13 |
| 40 | 39,92 | 1,174E-02 | 3,25E+07 | 1,00E+10 | 5,2 | 1,00E+10 | 1,88 | 66 | 6,60E-09 | 6,60E-13 |
| 41 | 30,29 | 1,458E-02 | 2,98E+07 | 1,00E+10 | 5,6 | 1,00E+10 | 2,33 | 54 | 5,40E-09 | 5,40E-13 |
| 44 | 25,34 | 1,678E-02 | 7,29E+07 | 1,00E+10 | 2,3 | 1,00E+10 | 2,68 | 55 | 5,50E-09 | 5,50E-13 |
| 45 | 20,53 | 1,979E-02 | 6,93E+07 | 1,00E+10 | 2,4 | 1,00E+10 | 3,17 | 40 | 4,00E-09 | 4,00E-13 |
| 46 | 14,59 | 2,584E-02 | 4,98E+07 | 1,00E+10 | 3,4 | 1,00E+10 | 4,13 | 14 | 1,40E-09 | 1,40E-13 |
| 47 | 10,76 | 3,270E-02 | 4,13E+07 | 1,00E+10 | 4,0 | 1,00E+10 | 5,23 | **4** | 4,00E-10 | 4,00E-14 |
| | | | | | | **Accumulated TID** | **22,33** | | | |

**Table 13: Dynamic Test Coolrunner CPLD-DUT5.**

The cross section obtained for functional errors in CR-II is shown the following graph:

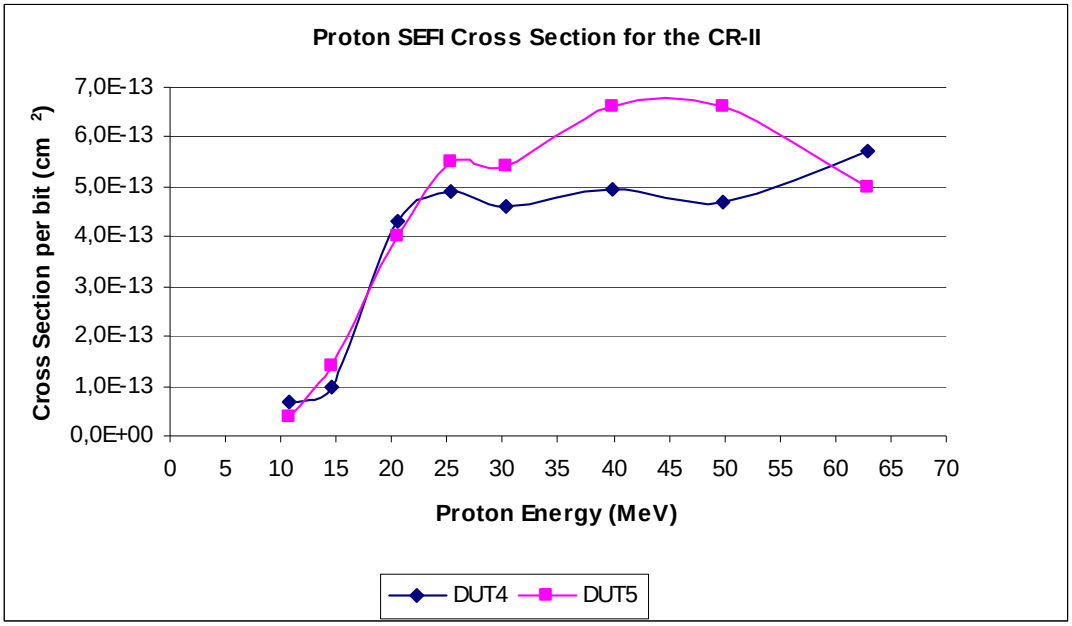


**Figure 26: Proton functional error cross-section for the CR-II .**

Data for cross section as function of proton energy can be used with CREME96 program introducing orbital parameters to get SEU and error rate predictions. We analyzed obtained data for a 680Km orbit and 98º (foreseen OPTOS orbit). Considering 100 orbits the results are showed bellow:

| Rates | SEUs/bit/second | SEUs/bit/day | SEUs/device/second | SEUs/device/day | **MTBF** (days) |
|---|---|---|---|---|---|
| DUT 1 | 1,02E-10 | 8,80E-06 | 1,02E-06 | 8,80E-02 | 11 |
| DUT 2 | 1,09E-10 | 9,42E-06 | 1,09E-06 | 9,42E-02 | 11 |
| DUT 3 | 7,98E-11 | 6,90E-06 | 7,98E-07 | 6,90E-02 | 14 |
| DUT 4 | 2,90E-11 | 2,51E-06 | 2,90E-07 | 2,51E-02 | 40 |
| DUT 5 | 2,83E-11 | 2,44E-06 | 2,83E-07 | 2,44E-02 | 41 |
| DUT 7 | 1,03E-10 | 8,94E-06 | 1,03E-06 | 8,94E-02 | 11 |

**Table 14: Data obtained from CREME96 for a 680Km LEO, with 98 º of inclination.**

### 4.2.7 TEST CONCLUSION

Taking into account the goals searched by this radiation campaign, it's a success that we can come up with responses for all the questions previously done. First of all, there has not been any latch-up during the whole test up to 63 MeV. Therefore we may conclude that CR-II is immune to SEL up to that energy. Although further heavy ion testing should be consider, the feeling is that quite similar results should be found.

We have tested Flash susceptibility to SEU even farther that what was previously expected in order to be sure that this memory is immune to proton particles up to 63 MeV. No SEU was register during the power on or off test. This has been a great success, because this means that we may recover from any situation with only a power cycle.

We have found the saturation cross section for protons at 30 MeV and a SEU threshold at 10 MeV. Even though this energies are quite low, when applying CREME96 to situate the device in a real space application, a 40 days time between failures has come up. Obviously CR-II

devices will not be suitable for critical systems, however they will be very useful for low duty cycle redundant systems, as the one exposed on section 6.

Finally, we have performed test over CR-II up to 22,33 Krads without any clue that pointed to a system degradation due to TID. After the proton test at PSI, Total Ionizing Dose test had been performed at CIEMAD, Madrid with gamma particles. CR-II power consumption and output impedances were monitor up to 30 Krad. No variation was detected.

### 4.2.8 TEST PERSONNEL

This test has been designed and performed by INTA and Universidad Carlos-III de Madrid

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# 5 LOGIC REDUNDANCY LEVEL. SEU CORRECTION THROUGH SELF-RECONFIGURATION

This approach presents an architecture for implementing radiation-hardened SoCs based on FPGAs. Previous works used Triple Module Redundancy (TMR) techniques together with scrubbing mechanisms based on partial reconfiguration. However, these solutions required external configuration controllers that increased the system complexity and deviated the design from the SoC principles. The proposed architecture uses novel self-reconfiguration techniques in order to eliminate the need for external components, so that a full radiation-hardened SoC can be implemented in a single FPGA. Since self-reconfiguration allows for on-board remote hardware updates, reliability is tackled at two key levels: Radiation-hardened operation and hardware upgradeability to solve design errors. Part of this work was presented on [MAR08] and is attached on Annex 2.

In order to achieve a Rad-Hard by design system, we must be able not only to mitigate the effects of SEU, but also to correct their effects on configuration memory. The mitigation is described in the following section. The correction technique using a self built-in module inside the FPGA will be described right bellow.

## 5.1 SEU MITIGATION

XTMRTool will be used to triplicate the whole design with Xilinx Triple Module Redundancy. Four problematic situations must be handled when triplicating the design:

### 5.1.1 Half Latches

A half latch is a weak keeper circuit connected to the chip enable input of every flip flop inside the FPGA. When a FF is not already configured by user to use that CE, the half latch is automatically activated. The following figure shows the half latch circuit:

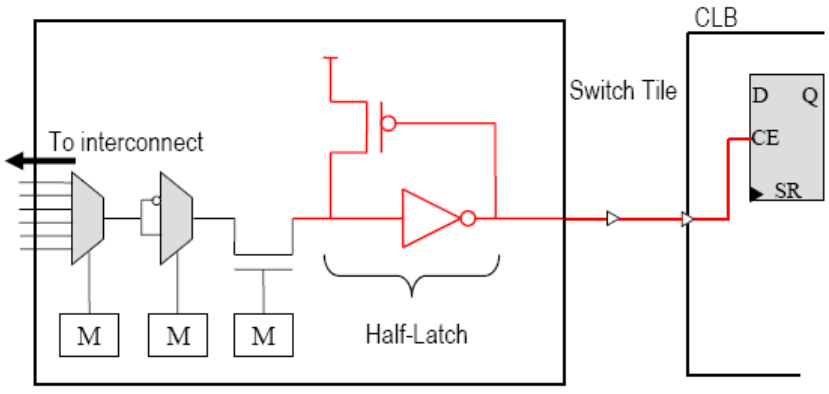



**Figure 27: Half Latch circuit.**

As HLs are not configured by the configuration memory, it is not possible to resolve the error by scrubbing methods. The HL will recover its initial state passed some time. The experience found when testing Virtex-II FPGA on the radiation chambers tell us that the time needed by HL to recover is bellow one second. Although, XTMRTool may be configured to extract HL from the design, exporting the unused signals from the FF to GND or VCC.

### 5.1.2 Logic

Device logic will be triplicated using XTMRTool macros. The tool automatically converts the simple design into a triplicated one.

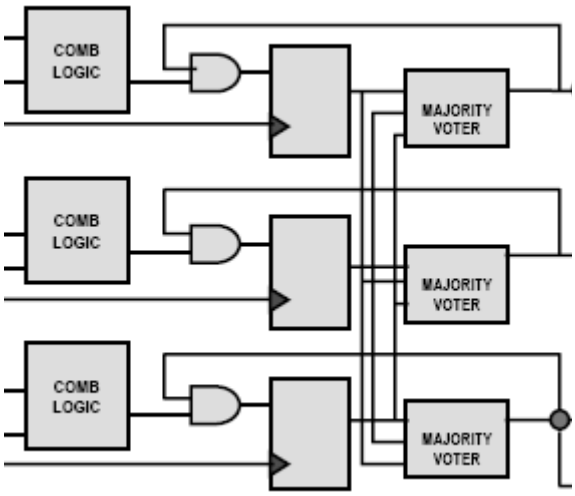
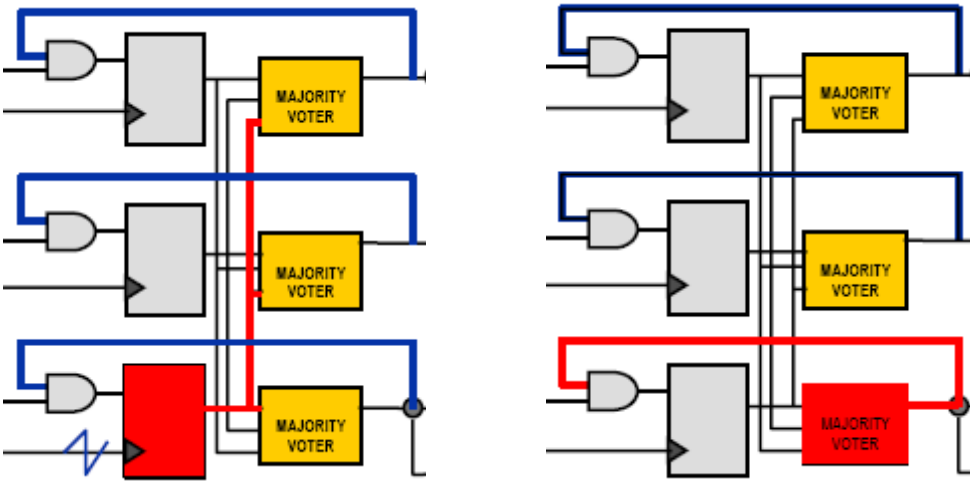



**Figure 28: Triplicated logic by XTMRTool.**

This method assures not single points of failure. Also the feedback voters allow the design to autonomously correct data paths errors. In **Error! Reference source not found.** we can see how the XTMR deals when an upset occurs in a data path. The redundant voters will correct the upset on the next FSM clock cycle:




(a) (b)

**Figure 29: (a) Autonomous upset correction. (b) Upset on majority feedback. Still two voters deliver the correct data.**

As in figure 22, if the outputs occur in the feedback voter, the output of that redundant module will be incorrect. The other two will still have valid data, and the upset must be corrected by reconfiguration.

### 5.1.3 Output Block

To assure not single point of failure on the outputs, it is necessary to triplicate each one and join three by three in the PCB trace. The following figure shows the XTMR output:

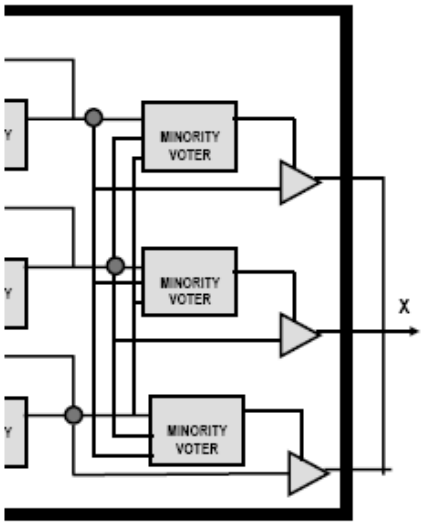
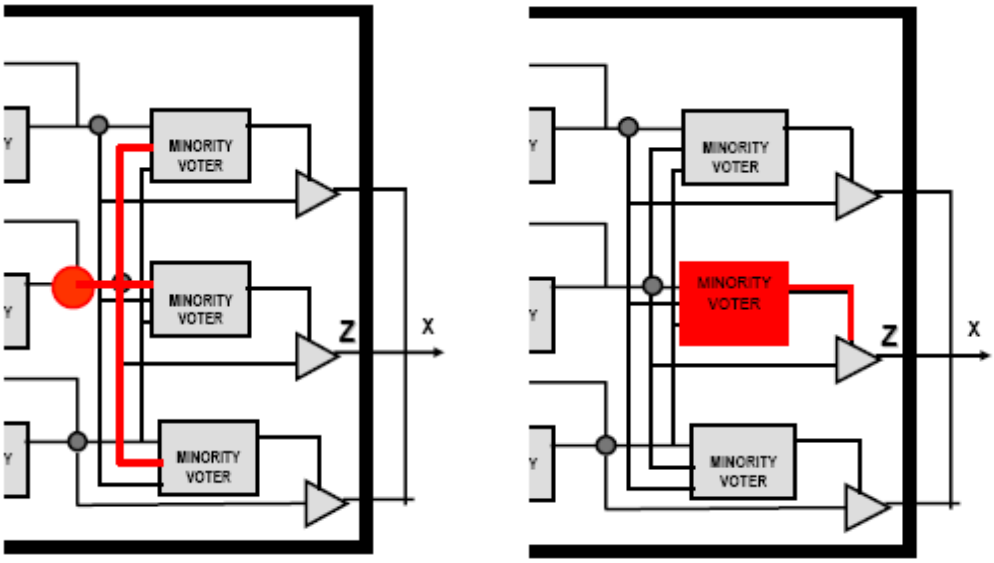



**Figure 30: XTMR Output block.**

It is very important, especially in high speed outputs, to make the connection outside the FPGA as close as possible to avoid timing glitches. With this configuration, two situations may occur. The first one is that a SEU hits the data path of one of the outputs. Then the minority voter which monitors the three output signal will deactivate the output driving it to high impedance (Figure 24). The second situation is that a SEU hits directly in one of the minority voters. This will deactivate the output, even though it is correct, however the two other outputs will still have the correct data (Figure 25).




(a) (b)

**Figure 31: (a) Minority voter detects the error and disconect the output. (b) SEU hits the minority voter.**

### 5.1.4 BRAM

BRAMs are changing modules that may not be scrubbed. Upsets in user block RAM can accumulate and must be monitored and corrected. Simple triplication of the block RAM is

often not enough. Therefore, an error detecting/correcting macro is needed to allow the FPGA to self correct the upsets that accumulate in block RAM. The block RAM self-correction algorithm [MIL08] is based on a custom macro replacing a group of block RAM primitives. This custom macro contains the block RAM scrubber engine and associated block RAMs described in VHDL.

The following figure shows a block diagram of the macro:

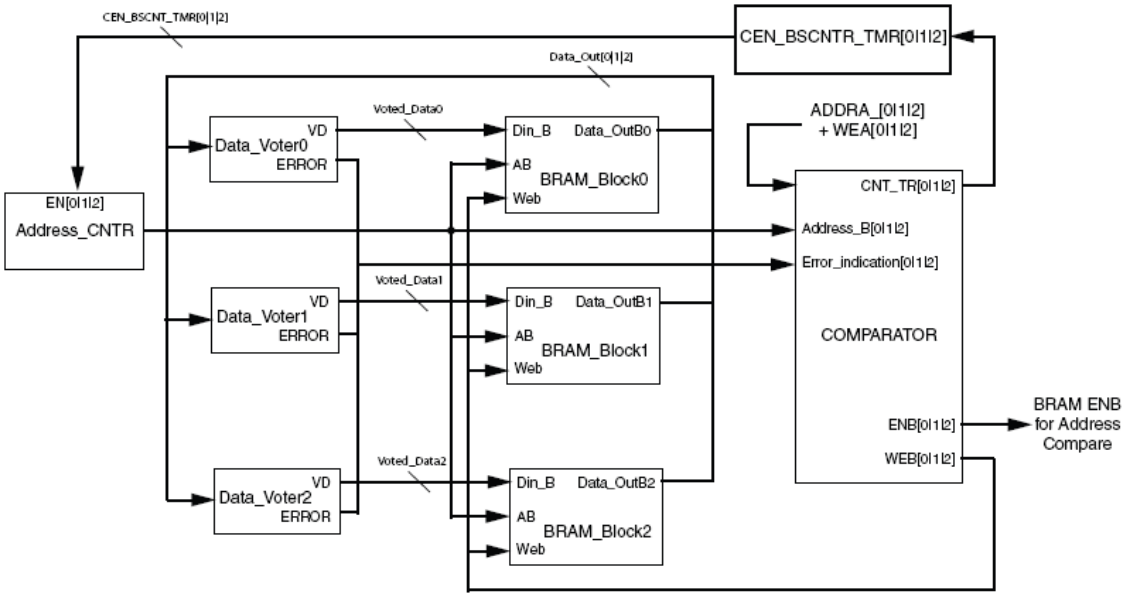



**Figure 32: Blocl RAM macro block diagram.**

The comparator module runs over all addresses of the triplicated BRAMs through the secondary port (b). Data out (Data_OutB) is then introduced inside the voters. If a mismatch occurs, an error signal is raised and the correct data is output off the voters (Voted_Data012) and presented on Din of the second port (b). When the comparator module detects the error signal, the counter is halted and a write cycle through the b-port is allowed. Ones the error has been corrected, the counter is enabled again and the infinite process continues running.

One of the drawbacks of this method is that no dual port RAMs could be used while the correcting macro is active. Also, an error may not be detected and corrected before a reading by the processor is performed, however the probability of this to happen might be insignificant.

## 5.2 SEU CORRECTION

The second approach is meant to correct SEUs in the configuration memory. Scrubbing [CAR08] will be used to avoid XTMR becoming useless because of the accumulation of bit-flips in the configuration memory. This technique uses partial run-time reconfiguration to continuously re-write the FPGA configuration. If any bit-flip has occurred, it will be solved when the bitstream is updated in the next reconfiguration cycle.

Unlike other previous approach [STU04], we have decided to include the scrubbing module inside the FPGA as part of the SoC. The module will be implemented as a custom peripheral named FPGA Hardener directly attached to the processor's bus. In our previous work on

[MAR08], this module was connected to the Internal Configuration Access Port (ICAP). However we now connect externally to the Select Map ports in order to reduce the SEU cross section of our system. This architecture provides two major advantages over previous approaches:

1. Hardware is simplified, because an external reconfiguration controller is no longer needed. Since the scrubbing module is connected to the SoC bus, the processor's non-volatile memory (Flash or EEPROM) may be also used to keep the scrubbing bitstream.
2. A door is opened to a novel on-board dynamic reconfiguration. As the proposed architecture already offers self-reconfiguration capabilities, new bitstreams could be loaded with a telecommand from Earth in order to correct faulty/outdated designs.

To prevent SEFI errors on SelectMap port or I/OB an external watchdog will monitor the FPGA Hardener. This watchdog must be reset periodically in order to check the aliveness of the internal module. Also, if a SelectMap SEFI is detected by the configuration module, a set signal must be activated. This external watchdog will then produce a 300ns down pulse in the PROG input of the FPGA, provoking a complete reconfiguration cycle. The following chart will show the external connections:

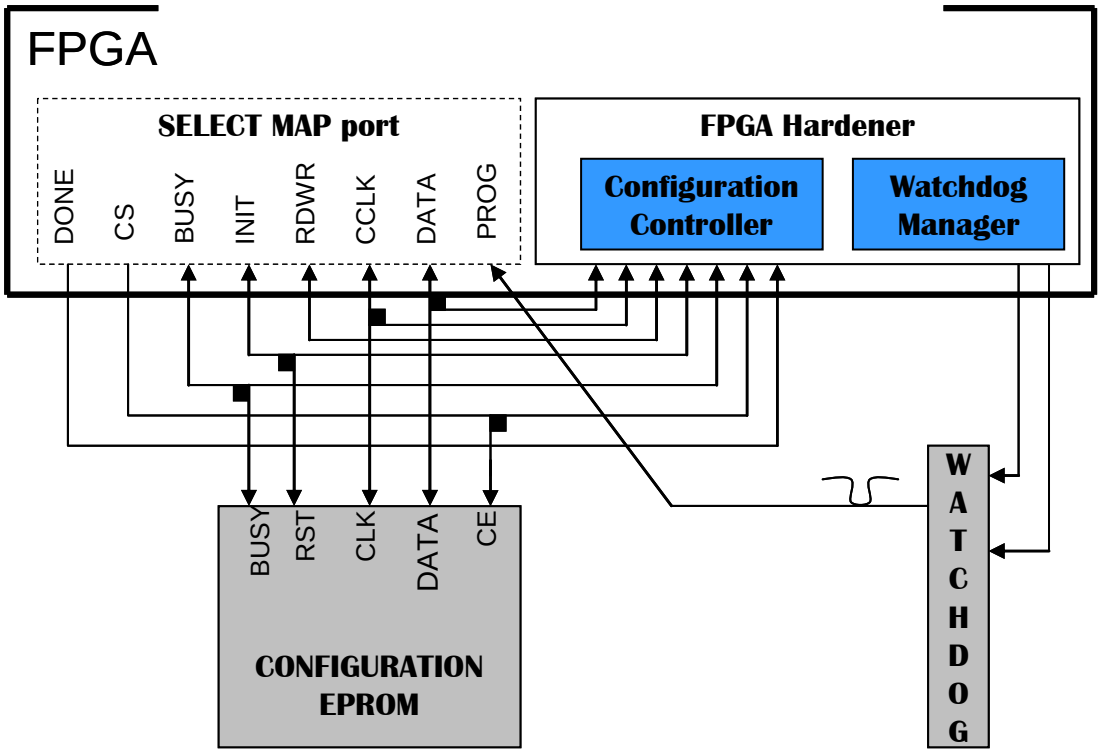



**Figure 33: External Connection to SMAP for Self Reconfiguration.**

### 5.2.1 Reconfiguration Cycle

It is very important to come up with the minimum reconfiguration frequency in order to minimize the possibility that there are two bit flips inside configuration memory at the same time. To be able to figure out this number we need to situate our system on a real space mission, so we can make a concrete radiation environment study. Taking into account the results of the radiation campaigns performed by the SEE Consortium members [SWI04-d], CREME96 simulator has been used to adapt the Virtex-II characterization to a typical five-year Low Earth Orbit (LEO) space mission. After applying CREME96 to the Virtex-II SEU

characterization on a real space orbit, we have found that we must foreseen 6.394 SEU/device/day

As noticed on [BRE08-b], SEU rates may be modeled as a Poisson process. For instance if the expected rate is 4 events per hour the probability of experiencing no upset is 0.018. Also the probability of experience 7 upsets is 0.06. The following graph shows a Poisson distribution for 4SEU/hour:

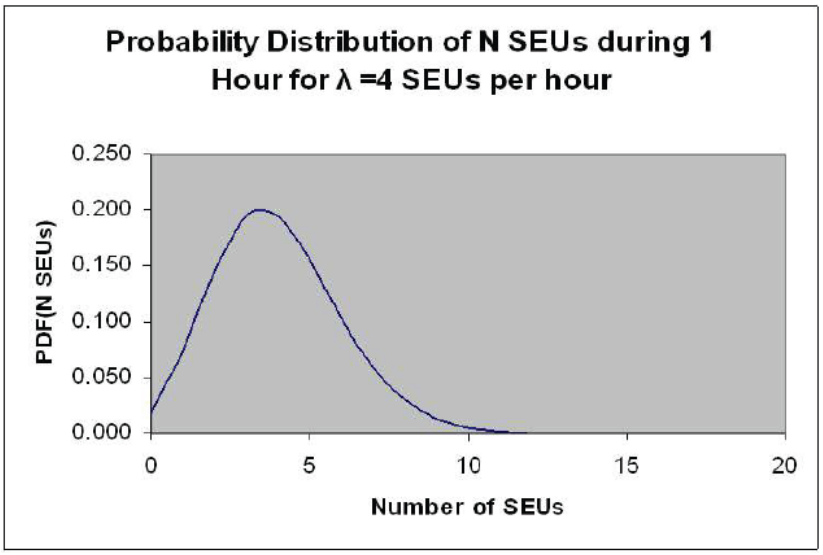



**Figure 34: SEU rate modeled as a Poisson process.**

Therefore, in order to minimize the risk of accumulating SEU on configuration memory, the minimum period for scrubbing cycles recommended should be ten times the expected SEU rate. Taking into account that the SEU rate is:

- 6.394 SEU/device/day => **1 SEU / 3.75 hour**.

Then the minimum scrub period is:

- 1 SEU / 3.75 hour / 10 => **1 scrub each 22' 30"**.

Of course any value below twenty two minutes and thirty seconds will lower the SEU accumulation probability.

## 5.3 SYSTEM ARCHITECTURE

A complete SoC architecture has been designed to support a typical On-Board Data Handling (OBDH) functionality. This system will be based on a MicroBlaze soft-processor, due to its easy integration with Xilinx FPGAs and its good area-performance ratio. Attached to it, the whole set of typical peripherals and interfaces needed by most On-Board Computers (OBC) will be included, such as MIL-STD-1553 Bus Controller, RS-422, timers, interrupt controllers, etc. The complete triplicated SoC is shown in the following block diagram:

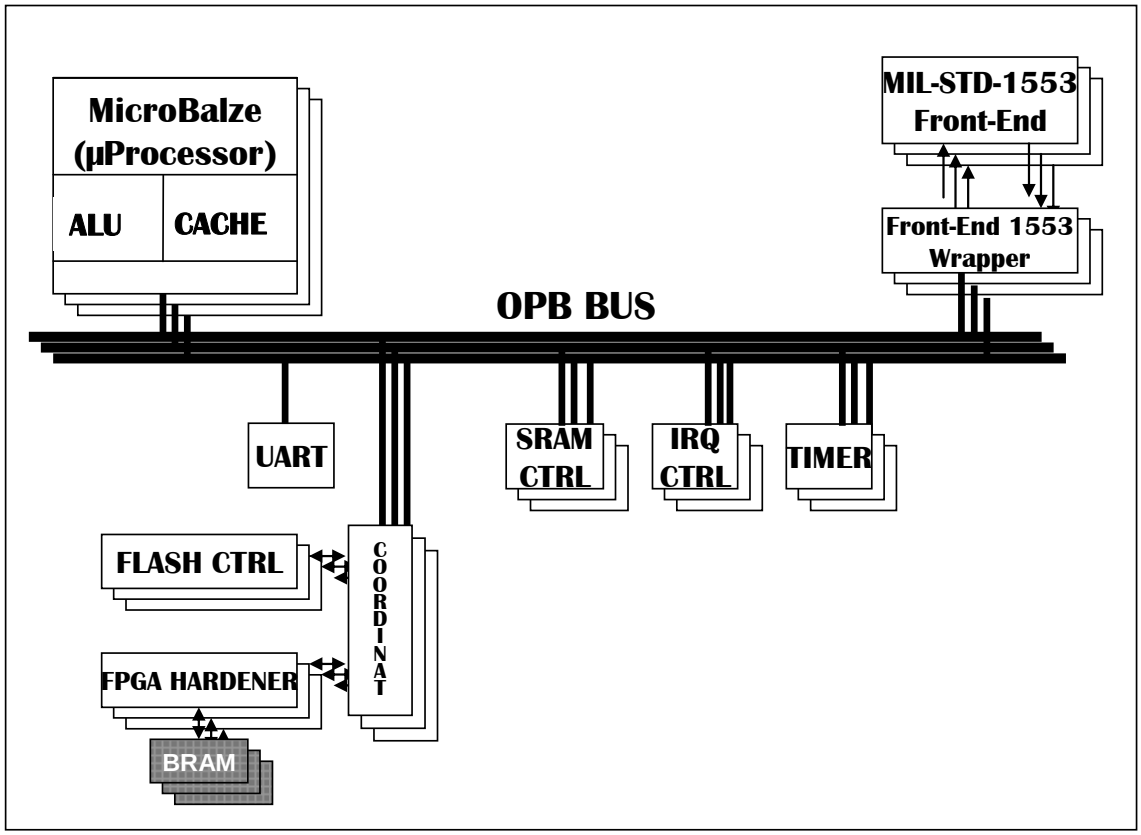



**Figure 35: XTMR SoC architecture block diagram**

In the upper chart the UART IP Core is not triplicated because it is not used for In-Flight mission but only with debug purpose during AIT.

The built-in scrubbing IP Core, so called "FPGA Hardener", is described in subsection bellow.

### 5.3.1 Built-in FPGA Hardener

The FPGA Hardener is a custom IP Core that will access flash memory to read the configuration bitstream, and then re-write frame to frame the FPGA configuration using the SelectMap external port. This process will assure the FPGA a good performance against SEU, correcting any possible bit-flip since the last scrubbing cycle. The FPGA Hardener has a low priority access the external Flash memory to avoid interference with On-Board Software. The FPGA Hardener will be directly connected the coordinator block, which is in charge of sharing the external Flash memory between the scrubbing module and the processor OPB bus.

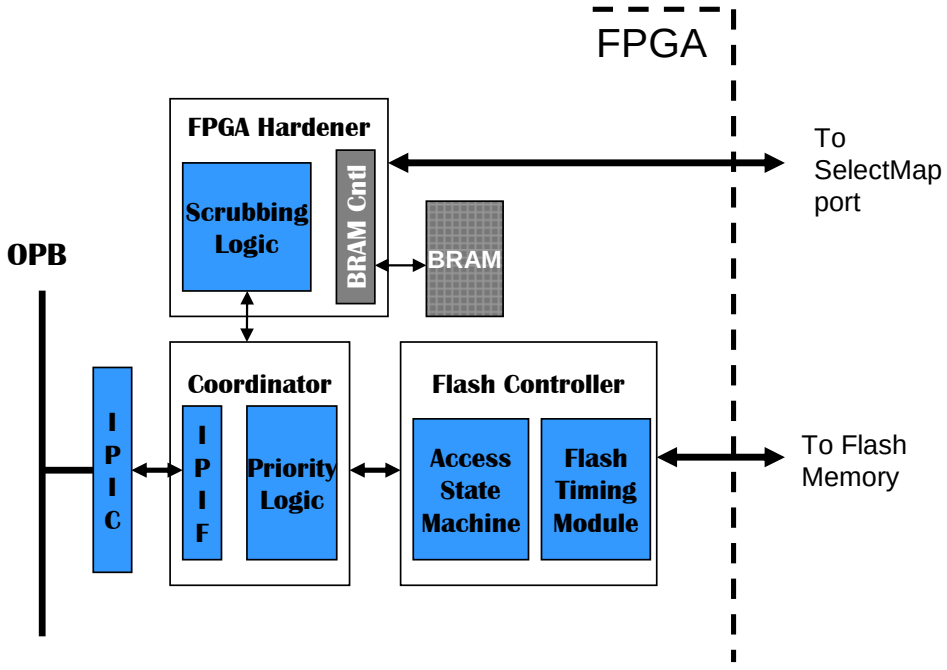



**Figure 36: FPGA Hardener and Flash Controller Block Diagram.**

Configuration bitstreams for Xilinx FPGAs are organized in frames of several thousand bits, 7872 in the case of a Virtex-II XQR2V6000. The minimum portion of bitstream that may be reconfigured is one frame. BlockRAM inside the FPGA Hardener will be used as an intermediate buffer to store frames before being sent to SelectMap port. Since Virtex-II BRAMs have 18Kbits, they have enough space for storing 2.29 frames of a XQR2V6000 device. Therefore, only one BRAM will be needed to implement this intermediate buffer.

# 6 DEVICE REDUNDANCY LEVEL. DISTRIBUTED ARCHITECTURE

The distributed architecture proposed is meant to be used in a real space mission. Taking advantage of the ultra low power CR-II tested, and the need of complex controls over several sub systems and instruments, a distributed architecture with several units achieving either common and independents duties is discussed.

To correctly understand the architecture philosophy is important to contextualize the system is which it will operate. A presentation of the project requirements is exposed here for a better understanding of the reader.

## 6.1 MISSION REQUIREMENTS AND PHILOSOPHY

OPTOS is conceptually a typical pico-satellite if taking into account its size (30 x 30 x 10 cm), its development time (2 years) and its cost. However, this type of satellite is usually developed by universities to have the chance of being involved in a real space project. In this case, this satellite aims to be a reusable platform for helping the industry and research centers to have the opportunity of testing either scientific or technological payloads in harsh space environment. Moreover, this platform must be a reliable and robust platform from the point of view of space environment (radiation tolerance, temperature and vacuum), attitude control (strong requirements established by a camera instrument) and satellite-Earth communications.

The following table resumes the most important mission requirements:

| | |
|---|---|
| Mission length | 2 years |
| Temperature range | -30 ºC to +40 ºC |
| Accumulated TID | 9 Krads @ year. |
| Orbit | Polar LEO |
| Max Power Budget | 1.0 Watt |
| Intra-Satellite Communications | CAN Bus |

**Table 15: OPTOS Mission main requirements.**

There are three mayor constraints that must be overcome to end up with a successful OBDH design:

1. Low cost in terms of device procurement.
2. Tight area limits.
3. Low power consumption due to reduce amount of solar cells.

Although OPTOS is a small satellite it has the same sub-systems (S/S) as a typical nano or micro-satellite. Also it is configured to support four different payloads (P/L). All these instruments need support from the OBDH in terms of analog inputs and outputs, digital interface and latch-up control to assure the healthiness of the whole satellite. OBDH shall provide up to 32 analog inputs, 3 analog outputs and more than 100 digital I/Os. This comprise the OBDH S/S to be much more complex than typical small satellites ones.

Because all these requirements, we propose the following OBDH architecture as the most suitable approach to success on this project.

## 6.2 OBDH ARCHITECTURE

The proposed architecture is based on a distributed processor where all terminals are connected by the CAN Bus. Each unit will be able to achieve redundantly all critical duties that belong to OBDH, and separately they will give their services to the S/S or P/L connected to them. Typical critical duties of an OBDH are: real time maintenance, self check supervision and P/L latch-up control. Additionally parallel processing may also been achieved if necessary. The purpose of this architecture is to distribute the criticism of the whole system, and to achieve globally the reliability of the system making each unit to work on its safest mode.

This design considers two kinds of units described here:

1. **Enhanced Processing Hardware (EPH):** This unit is based on Xilinx Virtex-II 1000 FPGA commanded by MicroBlaze soft-processor. The aim of this unit is to support the OBSW that will process communications through TTC S/S, and support ADCS software. These two S/Ss aim for a complex processing capability that may not be achieved by DOTs units.
2. **Distributed OBDH Terminals (DOT):** These units are based on ultra low power Xilinx CoolRunner-II 512 CPLD. They are oriented to control all the other satellite S/S (PDU, ADCS, etc) and P/Ls (GMR, ODM, FIBOS, APIS). The will be all interconnected (including EPH) through an optical wireless CAN Bus, and they will give support in terms of intelligent control logic through the following interfaces to the S/S and P/L connected to them:
    a. Four ten-bits ADC inputs with a dynamic range of 0 to 3.0V
    b. Sixteen digital inputs/outputs.

Prior to selecting these devices for its use in this mission, a complete study of literature about both was performed. In this master's thesis has been widely demonstrated the reliability of Virtex-II FPGA for non-critical space missions. This device has a average SEU failure rate on one every 3.75 hours. As will be explained later, a power cycle is performed every eclipse time, this is one hour power cycle. This will avoid cumulative SEU to appear. However, it is possible to have functional failures, but no probable. Although if it happens DOTs will keep critical duties working properly.

When looking for radiation literature for CR-II CPLD, the only thing we found was a Neutron[1] test performed by Xilinx. This test encouraged us to start a radiation campaign to check CR-II susceptibility to SEL and SEUs. This report was explained on section **Error! Reference source not found.**. As we plan to use these devices with a limited duty cycle, powering them on and off sequentially, and always keeping at least three devices up, a majority voter will always be possible to keep critical duties up and working.

Finally the purpose of this satellite is to create a reusable platform that will service to different operational P/L in the future. Therefore, the use of PLD guarantees a maximum

[1] Neutron testing is usually done to check devices behavioral on low energy Earth radiation. Neutrons are particles with energies of a few KeV.

upgradeability without having to change hardware design associated to the new instruments. This added to the fact that the PLDs to be used are more than one order of magnitude cheaper than any other Rad-Hard processor, make this distributed solution optimal for its implantation in OPTOS satellite.

The architecture proposed is shown in the following figure:

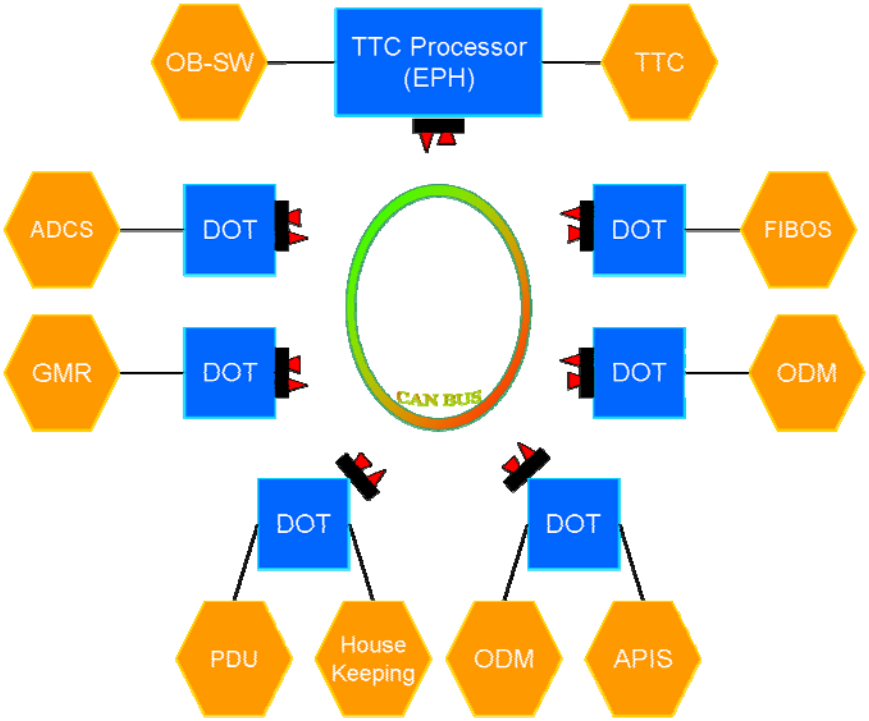



**Figure 37: OPTOS OBDH distributed architecture.**

A more deep explanation of each unit will be presented in the section bellow.

### 6.2.1 EPH

This unit is in charge of supporting OBSW S/S. It has direct link with communication S/S (TTC) through a serial synchronous interface, and with the rest of the OBDH through the wireless optical CAN. EPH is a so called SoC with a 32-bits soft-processor and several peripherals instantiated in it. Thanks to this, EPH has a high processing capability with reduced area and power consumption. The following figure shows a block diagram with the units holding the EPH circuit board:

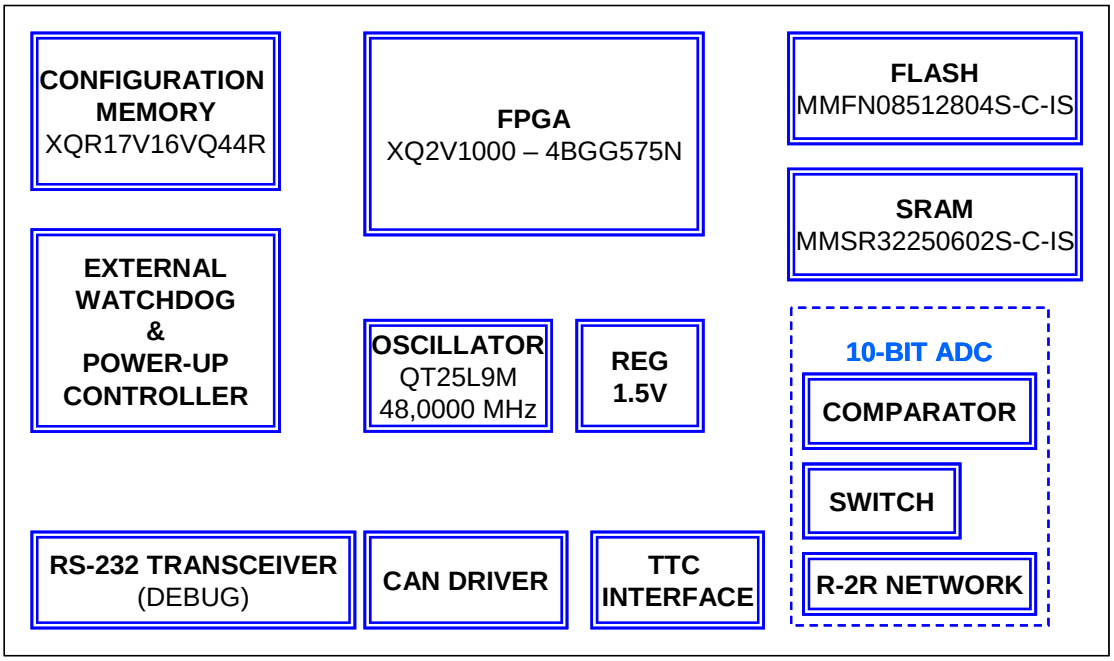



**Figure 38: EPH device block diagram.**

Its not the aim of this project to describe the components used except for those within the mitigation scheme. This is for instance the FPGA and the external watchdog.

#### 6.2.1.1 FPGA

As said before, the main mitigation scheme to be used inside the FPGA is a power cycle every eclipse period. This power down execution will be commanded by the internal OBSW, however we must assure that a non-recover status of the application (even though a software watchdog y also present) will not keep the device stacked for ever. To assure this, a triplicated internal module will be in charge of supervising the software and power off the device if not performed by OBSW in two consecutives eclipses. This module will communicate with OBSW using the secondary port of internal BRAM. The internal BRAM will be partially loaded at start-up with bootloader application that will get the OBSW from non-volatile Flash and charge it in external SRAM, were the OBSW will reside. The lasts addresses of this BRAM will be used to communicate with hardened power down supervisor. Here after there is a block diagram of the hardened module:

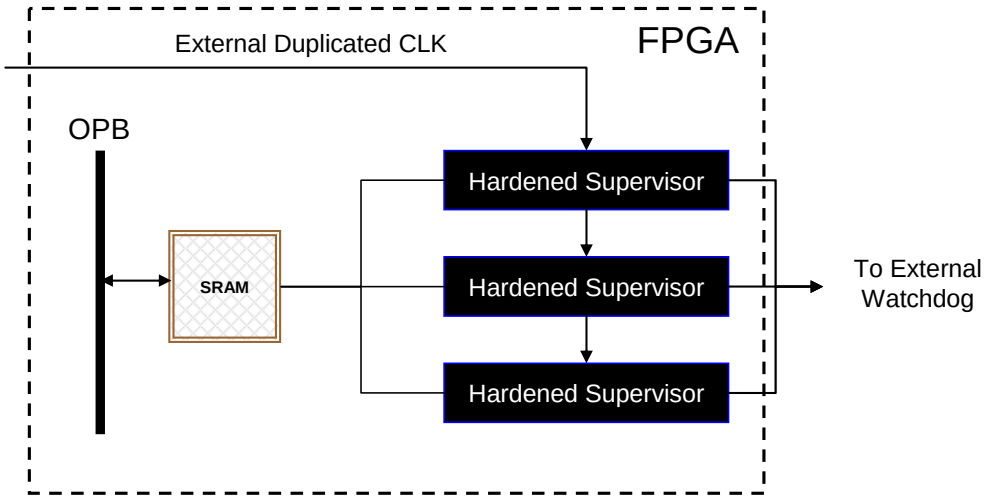



**Figure 39: Hardened power off supervisor.**

A complete visual description of the System on Chip design is shown in the next figure:

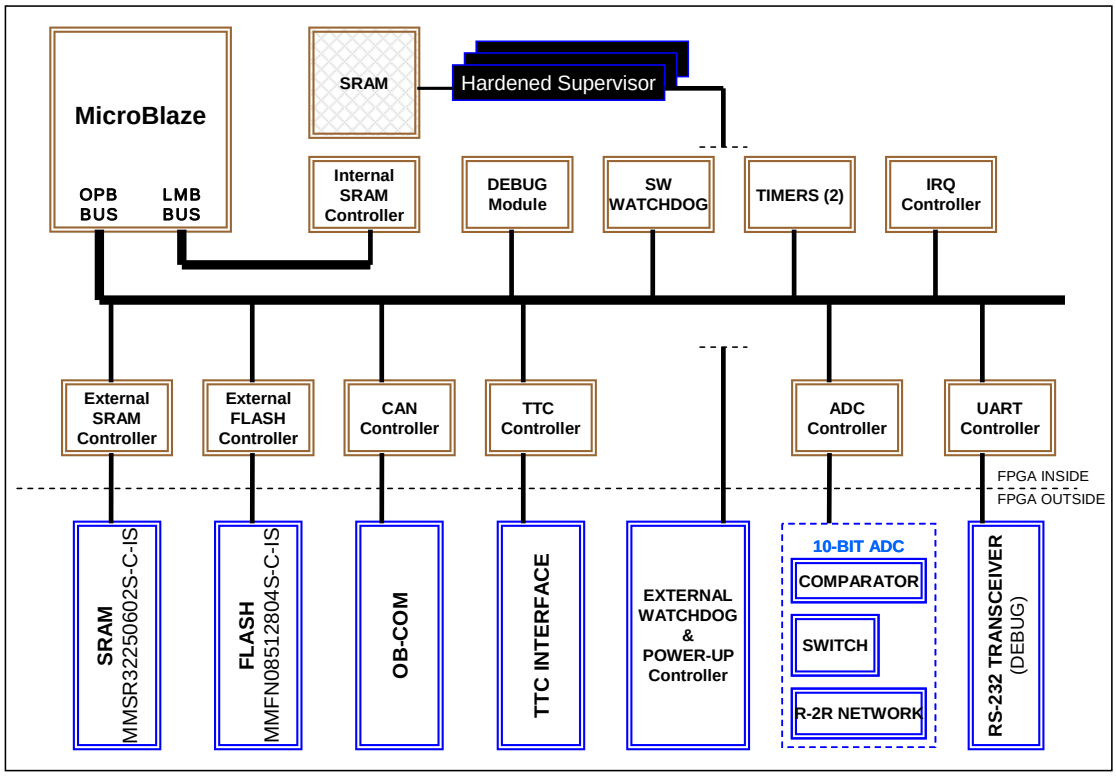



**Figure 40: SoC block diagram.**

The external watchdog is combined Rad-Hard logic of a typical timer watchdog and a power up system. This power up system is meant to hold the unit powered off during 10 minutes. In order to save power consumption during eclipse period, only DOTs will maintain the system running. During that period not attitude control, except by reaction wheel maintenance, will be performed. This is because with absence of solar sensor data no action might be done. House keeping telemetry will be acknowledged and stored by the other terminals in order to store it in telemetry mass memory when EPH is waked up.

### 6.2.1.2 DOT

This unit is divided in two mayor groups. First module named DOT_WD it's a complete Rad-Hard module to control the power on and power off the CPLD. This module will power up the CR-II and will maintain a watchdog timer that must be reseted by the CPLD every second to keep it powered. If the CPLD fails due to a SEU, then the external watchdog will power off the device, producing a new reconfiguration cycle the next time it's activated. An external counter is used to hold the unit off for a specific amount of time. This time will be variable for each DOT dependent of its characteristic duties. The second group (DOT_CPLD) it's the CPLD it self, with all the basic functions to attend the P/L and S/S connected to it, and to maintain critical OBDH duties.
Therefore, we can say that DOT_WD is a security assurance for correct any possible induced errors by radiation. While DOT_CPLD is the functional OBDH terminal.

The following block diagram shows a complete view of DOT unit:

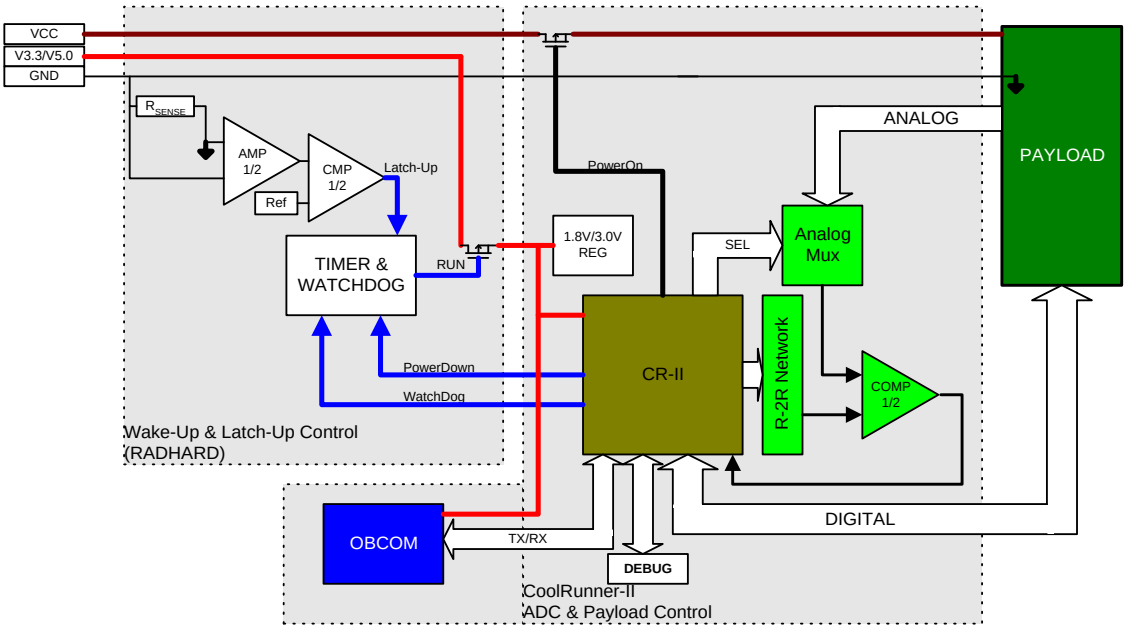



**Figure 41: DOT block diagram.**

Even though DOTs are commanded by a CPLD, they are quite complex units. DOTs competences are:

- Maintain the satellite real time. This process will be explained deeply here after.
- Receive commands from Earth through EPH to operate the P/L.
- Send the telemetries originated by P/L to be stored. While on eclipse period, keep those telemetries until EPH is powered up again,
- Send HK data from S/S to be stored. As well as P/L telemetries, HK must be stored during eclipse.
- Operate the different P/L.
- Operate ADCS S/S. This is, command the reaction wheel and the magneto torques on board.
- Dynamic latch-up sensing of P/L voltages. This latch-up sensing must be intelligence, because different P/Ls have different power consumption.
- Ephemeris propagation might be done to help ADCS software to keep them updated after eclipse period.

- Antennas deployment after launch.
- Camera shutter opening after launch.

The following chart shows the VHDL module description of CR-II:

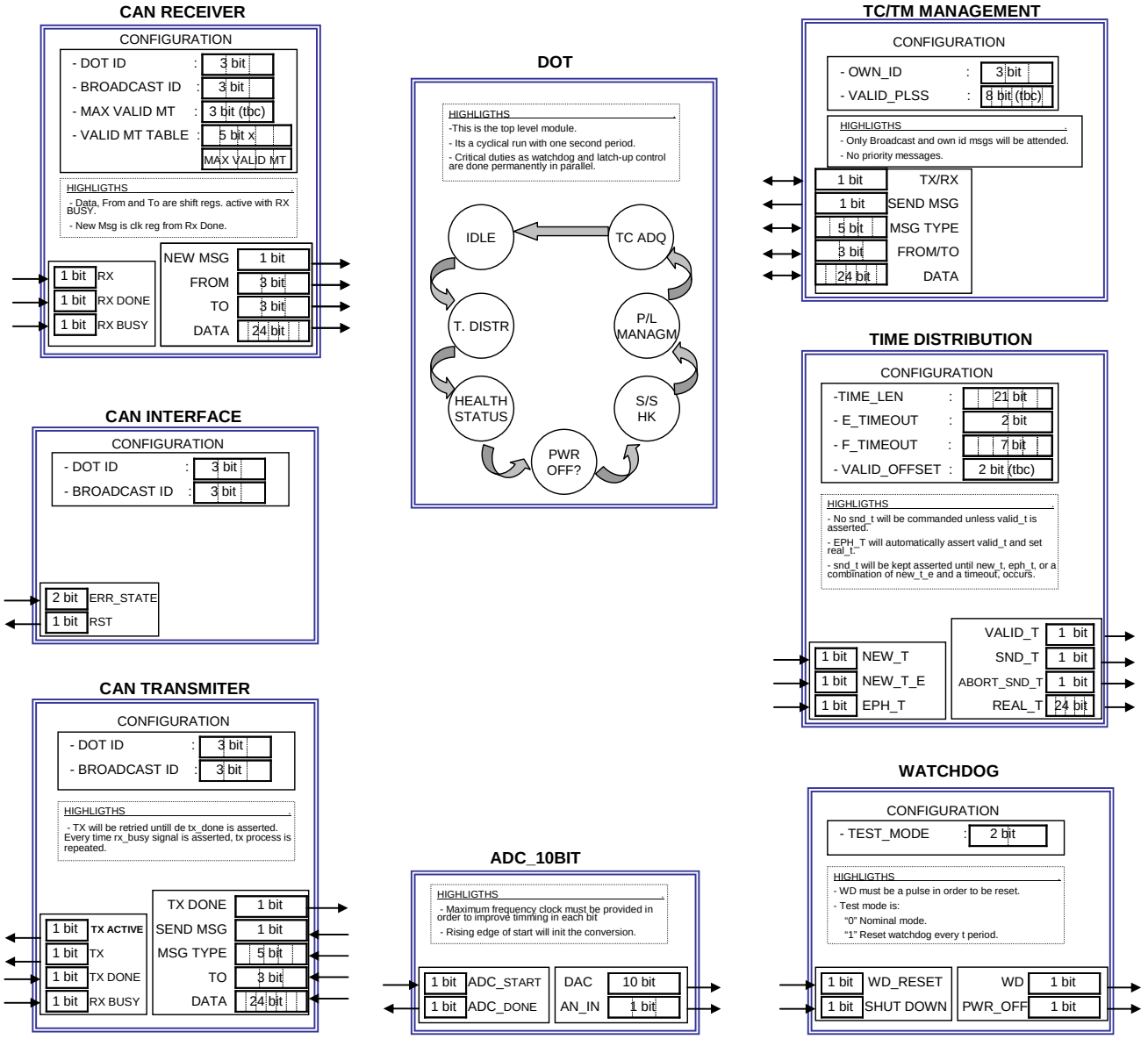



**Figure 42: DOT VHDL module definition.**

## 6.3 OPERATIONAL DESCRIPTION

The objective for using a distributed architecture is to achieve a reliable system without the need of using specific Rad-Hard components, as well as to increase modularity and reusability of the system. Nevertheless, this architecture must be transparent for the rest of S/S in order to facilitate their duties.

Every OBDH unit, EPH and DOTs, must be powered off periodically after a certain amount of time to be defined. This assures the integrity of each unit lowering the exposure time to radiation and assuring the recoverability in case of failure. With this methodology, we make sure that non unit will keep a functional failure indefinitely, assuring the system recovery in all cases.

OBDH will not be completely power off at no time. By design, it does assure that at least three units will be working at a time during the utile life of the satellite. This redundancy will allow to detect and correct error produced by SEUs. We also assure the correct maintainance of the satellite real time, which is a critical duty in order to execute the time tagged commands sent from Earth.

The distributed duties that must be achieved by OBDH are:

- **Data management:** each unit will be in charge of providing the necessary tools for data management of the P/L and S/S coupled to them. This is, each unit will provide the analogical (4) and digital (16) channels needed to acquire the data assuring its correct storage.
- **Storage:** OBDH will have in a distributed manner at least two units with storage capacity. All other units must deliver the data from their own S/S and P/L through the optical wireless communications on-board.
- **Power Control:** each unit is in charge of powering on and off its own P/L and S/S connected to it.
- **ADCS Management:** the attitude control management will be performed also distributed in-between EPH and three DOTs. EPH will be in charge of supporting the needed ADCD algorithms, while DOTs adjacents to the sensors (solar sensor and magnet) and actuator (reaction wheel and magneto torques) will operate them.
- **Real Time distribution:** because no particular unit will be powered up during the whole mission, an specific protocol has been developed in order to guarantee a correct management of the on-board real time. This protocol is described bellow.

### 6.3.1 REAL TIME MANAGEMENT

**Assumption:** each powered unit with a known real time (valid or not) will participate in the time distribution duty.

**Steps:**

1. EPH will be the one in charge of receiving the on-board real time when connecting with Earth. Once this time is updated, EPH will distribute this teal time to DOTs units with specific CAN message.
2. Every active unit will storage this time as the valid on-board real time.
3. From that point, with a 1 second period, each active unit will try to communicate the real time message in the CAN bus. Because of the intrinsic behavioral of CAN, only the unit with the highest priority will transmit firstly.
4. All other units will abort their own real time message as fast as the get it from any other unit. Then, they will compare their time with the one obtained. Depending on the result, two things will happened:
    a. The time is equal for each other unit. Then this time is validated and the real time period is ended until the next second.
    b. Some unit disagrees. Then that unit will send an erroneous real time message with its own real time. All other units will then send the same message with their own real time. A majority voting is then performed inside every unit. After this deterministic voting, every unit will gather the on-board real time.

This protocol will assure the time maintenance if EPH suffers a faulty behavior or shuts down during eclipse cycle. As said before, the time protocol will be active every second, however the time maintained is given in milliseconds magnitude, to avoid time shifts due to messaging delay. Time latency study for communication protocol has been performed in order to assure the consistency of the data timing.

### 6.3.2 COMMUNICATIONS TIME LATENCY

This subsection describes the maximum and minimum message transmission times from the point of view of the EPH to any P/L or S/S and vice versa.

#### 6.3.2.1 Telemetries Reception

Reception total time of a given message since the data is generated from a S/S of P/L might be defined as:

$$\mathbf{T_{Latencia} = T_{ini} + T_{CAN} + T_{rcp}}.$$

Where:

$\mathbf{T_{ini}}$ is the time that DOT takes to generate the message;
$\mathbf{T_{CAN}}$ is the propagation time of the message in the CAN bus;
$\mathbf{T_{rcp}}$ is the time that EPH takes to gather the message.

Taking into account the DOT clock cycle of 2 MHz, $\mathbf{T_{ini}}$ = 0,5 us.
Taking into account the EPH clock cycle of 48 MHz, $\mathbf{T_{rcp}}$ = 20,8 ns x # of instructions to store it in memory. An approximation of the # of instruction is given for the following process:

1. Interrupts the processor. (25 instructions)
2. Acknowledge the interruption. (10 instructions).
3. Store data is external SRAM memory. ( 30 instructions).

Total time for $\mathbf{T_{rcp}}$ = 20.8 ns x 65 = 1.352 us.

Finally, to figure out the propagation time we must consider the probability of message collision inside the bus. When you talk about collision in CAN bus, this is a unit trying to introduce a message when the bus is already in used. In that case, the unit must wait until that message ends, and also at any other units with a higher priority tries to send a message though CAN bus.

Assumptions:

1. The maximum number of units (DOTs + EPH) working at a time won't never be more than 8.
2. The maximum number of data to be transmitted is limited to 3 bytes. Therefore, when adding CAN preamble and tail to data, the maximum number of bits to be transmitted through the bus is 67 bits.
3. The CAN bus speed in this given design has been selected to 125 Kbps (8 us/bit).

Therefore, the maximum transmission time for a given CAN message is:

67 bits x 8 us/bit = 536 us. [1]

If the maximum number of messages to be sent in a given instant are 8 (maximum number of units):

$\mathbf{T_{CAN\_MAX}}$ = [1] x max_units = 536 us x 8 = 4.288 ms.

In the best case, the minimum number of messages to be sent is 1:

$\mathbf{T_{CAN\_MIN}}$ = [1] x min_units = 536 us x 1 = 0.536 ms.

Therefore, as $\mathbf{T_{ini}}$ y $\mathbf{T_{rcp}}$ are not significant (at least three orders of magnitude lower):

$$\mathbf{T_{Latencia}} = (\mathbf{T_{CAN\_MAX}} + \mathbf{T_{CAN\_MIN}}) / 2 \pm \Delta ((\mathbf{T_{CAN\_MAX}} + \mathbf{T_{CAN\_MIN}}) / 2), \mathbf{T_{CAN\_MAX}})$$

$$\mathbf{T_{Latencia} = 2.412\ ms \pm 1.876\ ms.}$$

#### **6.3.2.2** Telecommands Transmission

The formula to figure out the telecommands transmission is the same as the one for telemetries reception (see subsection 6.3.2.1). Therefore, latency time for telecommands is the same as for telemetries:

$$\mathbf{T_{Latencia} = 2.412\ ms \pm 1.876\ ms.}$$

# 7 CONCLUSIONS AND FUTURE WORK

The state of art and tests performed over SRAM based FPGAs has shown the strong interest inside the space community to get with reliable solutions to use this technology on harsh environments. As it always is, there is not a best configuration for every design. Each design has it's own peculiarities and requirements and therefore needs more specific solutions to come up with the most appropriate configuration. This master's thesis is a great example of that. In the distributed architecture approach presented here, has been demonstrated how this solution takes advantage of a complex system with several devices, using them to mitigate errors redundantly. This has allowed lowering the system total cost while achieving a great level of failure tolerance. In the other hand, a Rad-Hard by design complete System on Chip has been presented. Instruments and payloads with high computing needs, may take advantage of this proposal to improve by several orders of magnitude its tolerance to radiation environments.

Even though we have seen that right now is impossible to come up with a single chip solution completely immune to radiation because SEFI errors, we must take into account that its cross section is very low. For LEO or GEO orbits where heavy ions fluxes are so low, it will be quite rare to find one SEFI during a whole space mission, typically less than 15 years long.

Further work must be performed in the understanding of FPGAs internal configuration, to be able to come up with more effective solutions, taking into account banks differentiation, triple module domains separation, etc. The techniques proposed here must been improved taking into account Multiple Bits Upsets. The study of this phenomena and a good comprehension of it will allow develop enhanced techniques to avoid system failures.

One other thing of great interest for the author and the space community is the study of secure, hi-reliable solutions for On-Board reconfiguration. This technique will be a high add value to use SRAM FPGAs, allowing adding new hardware features and correcting design errors while on flight configuration.

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# ANNEX 1

# The Effects of Proton Irradiation on CoolRunner-II™ CPLD Technology

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***Abstract*— Nowadays, Complex Programmable Devices are highly demanded in space missions. In this sense, CoolRunner-II devices are very attractive due to their low-power consumption. However, there is no report on proton sensitivity for this technology until date. In this work proton irradiation tests were performed on these devices in the energy range from 6 to 63 MeV in both static and dynamic modes. The results reported allow considering these devices suitable for space applications.**

***Index Terms*— CPLD technology, proton irradiation effects, single event effect, single event upset, TID, test facilities**

## INTRODUCTION

The use of Complex Programmable Logic Devices (CPLD) has been traditionally restricted in circuits working in space or nuclear energy applications because of its susceptibility to radiation effects. The goal of this work is to evaluate the sensitivity to proton irradiation of Xilinx® CoolRunner-II™ CPLD (CR-II) technology [1]. This technology differs notably from conventional CPLD technology in that it is true CMOS and provides very low power consumption along with higher noise immunity and more possibilities in packaging. Although these devices are neither designed nor guaranteed to function in high radiation environments [2], they have interesting features for aerospace applications. In particular, OPTOS satellite project [3] is considering the use of CR-II devices to deal with very low power sub-systems and multiple redundant sensors.

Xilinx has already published results on CR-II radiation sensitivity for neutron related effects [4]. These results are important to characterize fault tolerance for devices working in atmospheric environments. When these devices are placed within space environment, proton and heavy ion irradiation tests must be also performed. Proton irradiation experiments on CR-II technology should consider its internal structure. This technology implements two configuration memories that enable *On-the-fly* reconfiguration and, therefore, small reconfiguration times. A non-volatile memory (Flash) stores configuration that can be downloaded onto volatile configuration memory (SRAM) every time the device is powered up or restarted. Although Flash memory devices have been thoroughly studied for working in space radiation environment [5] [6], proton testing is not very common. Furthermore, proton sensitivity of programmable devices with Flash configuration memories has been tested previously in few cases. We have found some reports on applications in space missions and in terrestrial experiments with high energy particles (ATLAS-LHC, *Large Hadron Collider* at CERN), [5]-[9]. On the other hand, there is a growing interest in the study and characterization of sensitivity of SRAM programmable devices with respect to different particles (neutrons, protons and heavy ions). Although this technology is not aimed for space applications, memory blocks and FPGA devices have been tested and results have been reported in several works, [10]-[12]. Even with these experimental results, irradiation experiments must be performed on CR-II devices in order to test their proton sensitivity. However, there is no report on proton sensitivity until date with this technology. The results provided in this paper demonstrate that these devices may be considered for its use in non-critical space missions without major hardening solutions, and to use them in critical missions with protection schemes is also possible.

## DEVICE TECHNOLOGY

CoolRunner-II technology is true CMOS not only in process technology but also in design technique. Instead of employing a sense amplifier for the product terms, configurable multiplexers are attached to the inputs of a CMOS NAND gate [1]. The avoidance of these sense amplifiers and the use of true CMOS technology imply a great reduction in power consumption, since no component is drawing current in standby state.

With respect to Fault Tolerance, CR-II devices present

three important sensitive areas that should be monitored and tested.

*Non-volatile Configuration Memory.* This memory keeps the configuration bitstream unchanged. Whenever the device is powered up, this bitstream is transferred onto volatile configuration memory.

*Volatile SRAM Configuration Memory.* This memory actually configures the device and describes its behavior. However, SRAM cells are deleted every time the device is powered down.

*Sequential Logic.* Although this part is SEU sensitive too, error probability is very low compared to configuration memory. Typically, the number of user flip-flops is 512 while configuration memory cells are around 290.000.

## EXPERIMENTAL DETAILS

Proton irradiation testing was performed in Paul Scherrer Institute (PSI), Laboratory for Astrophysics, at the Proton Irradiation Facility (PIF) components in the low energy area (NEB), [13]. This facility is member of European Component Irradiation Facilities (ECIF) supported by the European Space Agency (ESA). The energy available in the test facility ranges from 6 to 63 MeV, while proton flux can be up to $5 \cdot 10^8$ p/cm$^2$·s. The beam spot is a circle with a diameter up to 9 cm. The beam uniformity is 90% over a 5 cm diameter area. The flux dosimetry presents an accuracy of 5%.

Data presented in this paper were collected over an experiment carried out on February 14$^{th}$ 2007 on six samples (XC2C512-7PQG208C). All irradiation experiments take place in air. Figure 1 shows the five main subsystems developed for all different test performed to CR-II CPLDs. Irradiated devices are located in the Latch-Up Motherboard (LUM). As shown in Fig. 1, signals between Controller's Room and Ionization Chamber are sent through LVDS channels to ensure signal integrity through the 30 m distance. A PC Monitor System is used at Controller's Room to check real time information. An FPGA-based board (S3-Control board) is located 2 meters away from irradiated board. This board interfaces between LUM Board and PC Monitor, and also performs real time hardware check of DUT application

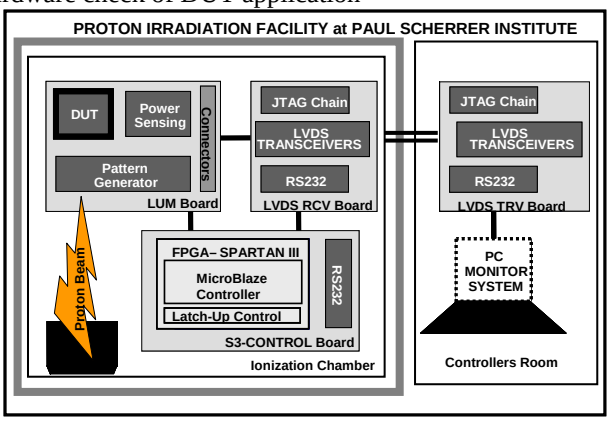



Figure 1. Test Setup inside Proton Irradiation Facility (PIF) at Paul Scherrer Institute.

*Latch-Up Motherboard* (LUM) contains the Device under Test (DUT) and it is located in front of the proton beam. DUT is mounted on a daughter board that may be easily inserted on and removed off the LUM board.

For the dynamic tests, a pattern generator is also included in the LUM board. It receives commands from S3-Control Board to start and stop running. It is implemented in a smaller CR-II device (XC2C128) located in the opposite corner from the DUT. Finally, results are checked in S3-Control Board.

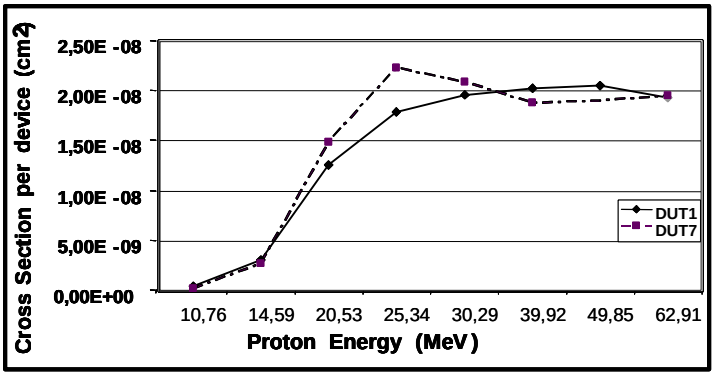
*S3-Control Board* is an evaluation board from AvNet with a Spartan-III FPGA commanded by a MicroBlaze microprocessor. A 50 pin connector is used for communications between LUM board and also between LVDS RCV Board. Also JTAG interface closes the complete JTAG chain consisting of the four programmable devices (Flash Configuration EEPROM (Spartan's), Spartan-III FPGA, CoolRunner-II 128, CoolRunner-II 512).

*Static Test*

The purpose of static test is to check the memory sensitivity, for this technology, when containing a configuration scheme. Initially both configuration memories contain the same scheme. Flash memory maintains configuration data, once stored, along successive power-offs and power-ons. On the other hand, SRAM memory maintains configuration data only while device is powered on.

CoolRunner-II devices are supposed to work in short time slots. Thus, continuous shut-downs and power-ons will be performed. Therefore, flash memory has been tested in these both states, in order to check the configuration data maintenance under harsh environments, while SRAM memory has been tested just in on-mode, as every time the device is powered on this memory is completely rewritten.

In this test, PC Monitor System performs periodical memory check of the DUT while under radiation. Continuous readbacks are performed during irradiation experiments in order to detect any change in Flash and SRAM configuration memories. Radiation test with the device powered down are also performed in order to check Flash memory TID in this mode. The device is changed quite often in order to avoid TID interfering in the SEU tests. No device was radiated over 22 kRad.



**Graph 1.** Proton SEU Cross-section for the CPLD (CR- II)

*Dynamic Test*

The purpose of this test is to check device sensitivity when running an application. As no reboot is performed during test, only SRAM configuration memory is analysed. Only a part of configuration bites is used for a given application; therefore, radiation results from this test will be better than for static test. The selected application must use a great part of device resources in order to obtain a representative measurement of technology susceptibility.

The application to be run in the DUT is a pipelined multiplier with two 10-bits operands and 20-bit result. The multiplier (5-stage pipelined) prototyped in the DUT uses almost all the resources available inside the tested device. The operands are generated by the Pattern Generator device that is commanded by the FPGA in the S3-Control Board. $2^{20}$ different multiplications are executed for every start command. The user can interact with the processor through the UART to start/stop the application and to receive real time data of the test status. For testing purposes, application is commanded by a 1 MHz clock. During the whole execution, the Spartan-III FPGA is checking multiplier results in order to detect any error. All errors are reported to the PC monitor with an interruption. When an error is detected, readback of SRAM configuration memory is performed in order to check the number of erroneous bits.

## EXPERIMENTAL RESULTS

Six CPLDs have been tested. Four of them (DUT1, DUT7, DUT2, DUT3) have been tested in static mode to characterize Total Ionization Dose (TID) and SEU sensitivity. DUT1 and DUT7 were irradiated powered on in order to test RAM memory. DUT2 and DUT3 were powered off and on respectively to test Flash memory in different conditions. Dynamic tests were carried out on DUT4 and DUT5.

1. *Static Test*

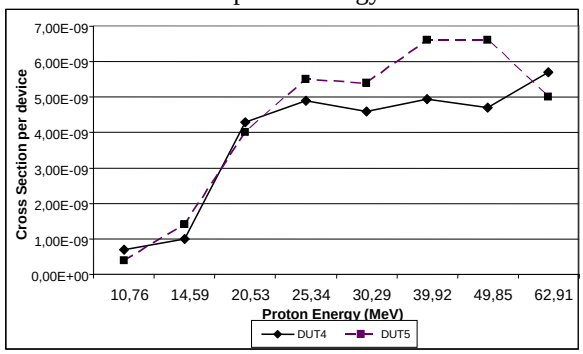
The aim of the test on DUT1 and DUT7 was measuring SEUs in SRAM. The results are shown in Table 1. Flash memory was also monitored but no SEU was observed. Although maximum fluence was programmed at 1E10 protons for each available proton energy, run was stopped when 100 upsets were registered in order to get 10% error in measurement [14].

In order to check Flash susceptibility, the fluence in DUT2 (powered off) was increased up to 1E10 (run 24) and 9E10 (run25), both at 62.91 MeV. No SEU was registered in DUT2 while powered off. This test is required for OPTOS application as CPLDs will be powered off several times during its working life. An additional run was made with the same device powered on just to confirm the SEU data for SRAM at 25MeV. The results for DUT2 and DUT3 (powered on) are shown in Table 2. Graph 1 shows cross-section as a function of proton energy for these tests.

2. *Dynamic Test*

DUT4 and DUT5 where tested under proton beam during normal operation. The running process was monitored and stored by the PC System through the S3-Control Board. Every time a SEFI (Single Event Functional Interrupt) was detected, the PC Monitor stored the data and reset the DUT to continue monitoring the effects of SEUs in the running application.

The results are shown in Table 3. Graph 2 shows cross-section as a function of proton energy for these tests.




**Graph 2**

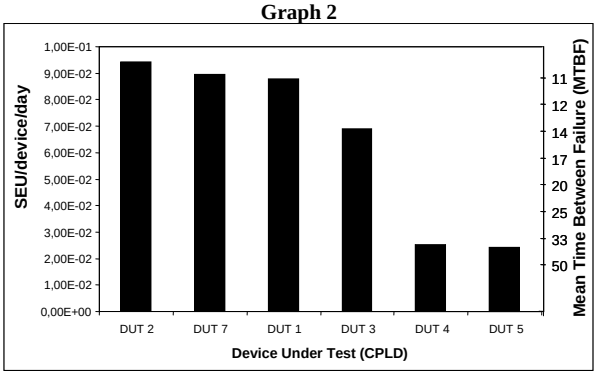



Figure 2**.** Expected proton SEE rate

3. *Test conclusions*

SEU and SEFI rate predictions are got from CREME96 code from cross section data (as a function of proton energy) and orbital parameters. We analysed the obtained data for a 680 km orbit and 98º (typical Low Earth Orbit). Considering 100 orbits the results are shown in Figure 2. This figure shows SEU and MTBF expected for DUTs in static tests (DUT2, DUT7, DUT1 and DUT3); as well as SEFIs and MTBFF for DUTs in dynamic tests (DUT4 and DUT5).

No parts failed from TID up to 22 kRad. No Single Event Latch-up was detected for proton energies up to 63MeV and fluences around $10^{10}$ protons/cm$^2$. Cross-section did not increase for proton energies greater than 30 MeV (Saturation Cross-section), while proton energy threshold is less than 10MeV.

No SEU was observed in the whole test inside Flash memory, neither when the DUT was powered-on nor powered-off.

## CONCLUSIONS

CR-II devices present an ultra low power consumption and wide configurability. This makes them very suitable for self powering sensors and small format subsystems. As described previously, no SEE has been detected in

Flash memory at any time during the tests. This is very good news, as it means that an application may be recovered at any time by powering off and on the device.

Regarding volatile memory sensitivity we have found (Graph. 1) that SRAM cells are quite sensitive to protons with energies greater than 15 MeV. However, according to data obtained from CRÈME 96 (Figure 2), an MTBF of 11 days is expected in the worst case. In real applications, the MTBFF will be several times higher, since only a fraction of the SEUs will produce a functional failure.

Taking into account that lots of applications do not need to be running all the time, it is possible to reboot CR-II whenever it is on IDLE state. In the scope of the OWLS project [15], housekeeping is intended to become wireless. On every satellite there are thousands of temperature sensors that might be shut down several times every second. For this kind of application the probability of failure is very low. Thus, CR-II may not be suitable for use within critical applications, but it may be a great choice for non-critical ones.

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| Device | RUN | Energy (MeV) | LET (MeV /mg/cm$^2$) | Flux (p/cm$^2$/s) | Fluence (p/cm$^2$) | Maximum Fluence (p/cm$^2$) | TID (krad) | SEU (SRAM) | Cross Section per device (SRAM) |
|---|---|---|---|---|---|---|---|---|---|
| DUT1 | 2 | 62,91 | 8,259E-03 | 1,00E+07 | 5,17E+09 | 1,00E+10 | 0,68 | **100** | **1,93E-08** |
| | 4 | 49,85 | 9,879E-03 | 5,87E+07 | 5,18E+09 | 1,00E+10 | 0,82 | **106** | **2,05E-08** |
| | 5 | 39,92 | 1,174E-02 | 4,24E+07 | 4,96E+09 | 1,00E+10 | 0,93 | **100** | **2,02E-08** |
| | 6 | 30,29 | 1,458E-02 | 3,09E+07 | 5,16E+09 | 1,00E+10 | 1,20 | **101** | **1,96E-08** |
| | 7 | 25,34 | 1,678E-02 | 2,03E+07 | 5,69E+09 | 1,00E+10 | 1,53 | **102** | **1,79E-08** |
| | 9 | 20,53 | 1,979E-02 | 4,12E+07 | 7,95E+09 | 1,00E+10 | 2,52 | **100** | **1,26E-08** |
| | 6 | 14,59 | 2,584E-02 | 3,51E+07 | 1,00E+10 | 1,00E+10 | 4,13 | **31** | **3,10E-09** |
| | 15 | 10,76 | 3,270E-02 | 7,01E+07 | 1,01E+10 | 1,00E+10 | 5,28 | **5** | **4,95E-10** |
| | **Accumulated TID** | | | | | | **17,10** | | |
| DUT7 | 17 | 62,91 | 8,259E-03 | 3,32E+08 | 6,30E+09 | 1,00E+10 | 0,83 | **123** | **1,95E-08** |
| | 18 | 39,92 | 1,174E-02 | 1,92E+08 | 5,96E+09 | 1,00E+10 | 1,12 | **112** | **1,88E-08** |
| | 19 | 30,29 | 1,458E-02 | 1,50E+08 | 5,40E+09 | 1,00E+10 | 1,26 | **113** | **2,09E-08** |
| | 20 | 25,34 | 1,678E-02 | 1,20E+08 | 5,06E+09 | 1,00E+10 | 1,36 | **113** | **2,23E-08** |
| | 21 | 20,53 | 1,979E-02 | 1,12E+08 | 6,69E+09 | 1,00E+10 | 2,12 | **100** | **1,49E-08** |
| | 22 | 14,59 | 2,584E-02 | 8,61E+07 | 1,01E+10 | 1,00E+10 | 4,18 | **28** | **2,77E-09** |
| | 23 | 10,76 | 3,270E-02 | 7,13E+07 | 1,01E+10 | 1,00E+10 | 5,28 | **3** | **2,97E-10** |
| | **Accumulated TID** | | | | | | **16,15** | | |

Table 1. Static Test CoolRunner-II Powered on

| Device | RUN | Energy (MeV) | LET (MeV/ mg/cm$^2$) | Flux (p/cm$^2$/s) | Fluence (p/cm$^2$) | Time (s) | Maximum Fluence (p/cm$^2$) | TID (krad) | SEU (SRAM) | SEU (Flash) | Cross Section per device (SRAM) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DUT2 | 24 | 62,91 | 8,259E-03 | 3,58E+08 | 1,04E+10 | 29 | 1,00E+10 | 1,37 | | **0** | |
| | 25 | 62,91 | 8,259E-03 | 3,66E+08 | 9,04E+10 | 247 | 9,00E+10 | 11,95 | | **0** | |
| | 26 | 25,34 | 1,678E-02 | 1,16E+08 | 4,74E+09 | 41 | 1,00E+10 | 1,27 | **107** | | **2,26E-08** |
| | | | | | **Accumulated TID** | | | **14,59** | | | |
| DUT3 | 27 | 62,91 | 8,259E-03 | 3,71E+08 | 1,00E+11 | 4,5 | 1,00E+11 | 13,21 | **2341** | **0** | **2,34E-08** |

Table 2**.** Static Test CoolRunner-II

| Device | RUN | Energy (MeV) | LET (MeV/ mg/cm$^2$) | Flux (p/cm$^2$/s) | Fluence (p/cm$^2$) | Time (s) | Maximum Fluence (p/cm$^2$) | TID (krad) | SEFI | Cross Section per device |
|---|---|---|---|---|---|---|---|---|---|---|
| DUT4 | 29 | 62,91 | 8,259E-03 | 7,00E+07 | 1,00E+10 | 2,4 | 1,00E+10 | 1,32 | 57 | 5,70E-09 |
| | 30 | 49,85 | 9,879E-03 | 5,59E+07 | 1,00E+10 | 3,0 | 1,00E+10 | 1,58 | 47 | 4,70E-09 |
| | 31 | 39,92 | 1,174E-02 | 4,14E+07 | 1,01E+10 | 4,1 | 1,00E+10 | 1,90 | 50 | 4,95E-09 |
| | 32 | 30,29 | 1,458E-02 | 3,12E+07 | 1,00E+10 | 5,4 | 1,00E+10 | 2,33 | 46 | 4,60E-09 |
| | 33 | 25,34 | 1,678E-02 | 2,56E+07 | 1,00E+10 | 6,6 | 1,00E+10 | 2,68 | 49 | 4,90E-09 |
| | 34 | 20,53 | 1,979E-02 | 2,29E+07 | 1,00E+10 | 7,3 | 1,00E+10 | 3,17 | 43 | 4,30E-09 |
| | 35 | 14,59 | 2,584E-02 | 1,74E+07 | 1,00E+10 | 9,6 | 1,00E+10 | 4,13 | 10 | 1,00E-09 |
| | 36 | 10,76 | 3,270E-02 | 1,40E+07 | 1,00E+10 | 12,0 | 1,00E+10 | 5,23 | **7** | 7,00E-10 |
| | | | | | **Accumulated TID (DUT4)** | | | **22,33** | | |
| DUT5 | 38 | 62,91 | 8,259E-03 | 5,88E+07 | 1,00E+10 | 2,9 | 1,00E+10 | 1,32 | 50 | 5,00E-09 |
| | 39 | 49,85 | 9,879E-03 | 4,97E+07 | 1,00E+10 | 3,4 | 1,00E+10 | 1,58 | 66 | 6,60E-09 |
| | 40 | 39,92 | 1,174E-02 | 3,25E+07 | 1,00E+10 | 5,2 | 1,00E+10 | 1,88 | 66 | 6,60E-09 |
| | 41 | 30,29 | 1,458E-02 | 2,98E+07 | 1,00E+10 | 5,6 | 1,00E+10 | 2,33 | 54 | 5,40E-09 |
| | 44 | 25,34 | 1,678E-02 | 7,29E+07 | 1,00E+10 | 2,3 | 1,00E+10 | 2,68 | 55 | 5,50E-09 |
| | 45 | 20,53 | 1,979E-02 | 6,93E+07 | 1,00E+10 | 2,4 | 1,00E+10 | 3,17 | 40 | 4,00E-09 |
| | 46 | 14,59 | 2,584E-02 | 4,98E+07 | 1,00E+10 | 3,4 | 1,00E+10 | 4,13 | 14 | 1,40E-09 |
| | 47 | 10,76 | 3,270E-02 | 4,13E+07 | 1,00E+10 | 4,0 | 1,00E+10 | 5,23 | **4** | 4,00E-10 |
| | | | | | **Accumulated TID (DUT5)** | | | **22,33** | | |

Table 3. Dynamic Test CoolRunner-II

# ANNEX 2

## Radiation Hardening of FPGA-based SoCs Through Self-Reconfiguration and XTMR Technique

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**ABSTRACT**

SRAM-based FPGAs are increasingly being used in space applications. However, there are still many concerns about the reliability of these devices in high-radiation environments, particularly due to the possibility of Single-Event Upsets (SEUs) in the configuration memory. This paper presents an architecture for implementing radiation-hardened SoCs based on FPGAs. Previous works used Triple Module Redundancy (TMR) techniques together with scrubbing mechanisms based on partial reconfiguration. However, these solutions required external configuration controllers that increased the system complexity and deviated the design from the SoC principles. The proposed architecture uses novel self-reconfiguration techniques in order to eliminate the need for external components, so that a full radiation-hardened SoC can be implemented in a single FPGA. Since self-reconfiguration allows for on-board remote hardware updates, reliability is tackled at two key levels: Radiation-hardened operation and hardware upgradeability to solve design errors.

### INTRODUCTION

The use of FPGAs in high-radiation environments is not yet well accepted by many people inside the space market [1], but there is an increasing interest in these devices due to the improved cost efficiency and the lower development time in comparison to other design options such as ASICs or discrete logic. The most serious drawback of PLDs in space applications comes from the fact that SEUs may alter the configuration memory of SRAM-based FPGAs. To avoid this issue, Xilinx developed a technique based on a continuous FPGA reconfiguration [2], which is commonly known as scrubbing. This mechanism is usually complemented by classic TMR techniques to prevent errors on user flip-flops. Users do not need to implement TMR by themselves, applications such as Xilinx TMRTool [3] can be used to automatically harden an existing design.

Another important advantage of SRAM-based FPGAs is their capability of being in-system reconfigured. This feature is especially important in space applications, because it allows modifying on-board hardware by replacing faulty/outdated FPGA bitstreams at different stages of a mission [4]. Some example uses are: rectification of design faults, improvement of processing algorithms, alteration of system functionality in response to changed mission requirements, modification of hardware configurations to reduce power characteristics, etc.

FPGA reconfiguration can be static or dynamic. The former requires that the system has to be stopped and rebooted when its FPGAs are reconfigured. The latter allows for the system to continue running during reconfiguration. All modern (since Virtex family) Xilinx FPGAs support dynamic reconfiguration through run-time partial reconfiguration, that is, part of the device can be reconfigured while the rest of it continues its normal operation. The most compelling mode of dynamic reconfiguration is self-reconfiguration, where the FPGA itself changes part of its configuration at run-time [5]. Virtex-II devices, as well as Virtex 4 and 5, provide the Internal Configuration Access Port (ICAP), an internal configuration interface specifically designed to enable self-reconfiguration.

In the following section, a brief overview about radiation effects is provided. Section 3 details a methodology for SEU mitigation. Section 4 describes the proposed architecture for radiation-hardened FPGA-based SoCs. Next, section 5 discusses the reconfiguration cycles needed to avoid SEUs. Finally, section 6 presents the conclusions.

## RADIATION EFFECTS

Several FPGA vendors already provide radiation tolerant devices, immune to Single Event Latch-ups (SELs) and capable of withstanding high Total Irradiation Doses (TIDs). Moreover, non-reconfigurable devices based on One Time Programmable (OTP) technologies have achieved very good immunity to SEUs.

However, SEUs are still a major concern in SRAM-based FPGAs, even in radiation-hardened devices. Fortunately, FPGA-oriented SEU mitigation techniques have been significantly improved in the recent years, mainly due to manufacturers' efforts. The following subsection summarizes the existing literature for Xilinx Virtex-II, a device capable of implementing the architecture proposed in this paper.

### Previous Studies

Because of the complexity of current programmable logic devices, it is very difficult to determine the sensitivity of a FPGA-based system to SEUs. According to [6], there are two approaches to SEU testing, static and dynamic. Static SEU testing only determines the sensitivity of each memory element, without observing the effects on the functionality of the application. Dynamic SEU testing takes into account the functionality of the circuit implemented in the FPGA. The static SEU characteristic of Virtex-II devices can be easily measured using configuration readback, which returns the state of most storage cells of the device: Configuration bits, BlockRAM and user flip/flops. Based on testing made in [7]:

- SEU cross section is $3.8 \times 10^{-8}$ $cm^2$/bit for Heavy Ions (HI) with a effective LET of 142 MeV and up to $5.8 \times 10^3$ ion/$cm^2$.
- SEU cross section is $3.7 \times 10^{-14}$ cm2/bit for Protons ($p^+$) of up to 198 MeV, flux greater than $10^9$ particles/($cm^2 \cdot s$) and fluencies of $10^{11}$ $p^+/cm^2$.

These results show that the SEU sensitivity of Virtex-II devices should be considered high. Although static testing provides a valuable indication of the SEU sensitivity of the device, what designers need to know is the actual effect of SEUs in their systems. In particular, what has to be demonstrated is the usability and reliability of the FPGA in space environments. It is therefore necessary to characterize the behavior of the applications implemented in the FPGA when SEU mitigation techniques are being applied.

Several studies have been performed over Radiation Tolerant Virtex-II designs using both TMR and scrubbing techniques for SEU mitigation. In [8], Saab Ericson Space (under ESA contract) performed several tests to Virtex-II FPGAs, implementing different designs and using different TMR techniques from Xilinx (XTMR_v1 and XTMR_v2). This document concludes that using XTMR as a mitigation technique greatly improves the device cross section for Single Event Functional Interrupts (SEFIs). But not only that, the test performed by the Jet Propulsion Laboratory (JPL) [7] states that "*it was never observed that only a part of the device had a failure that couldn't be repaired by the scrubbing of the configuration bits (Stuck Error)*". This JPL test concludes that when both mitigation methods, TMR and scrubbing, are implemented together, the design appears to be essentially immune to functional errors.

## SEU MITIGATION PROPOSAL

This section describes the SEU mitigation methodology used to by the proposed Rad-Hard By Design (RHBD) SoC architecture. As stated in [9], to achieve the best results we must use a prevention method combined with error correction method. A complete description of this architecture can be found on section 4.

### SEFI Prevention

Two main combined approaches have been designed to harden the FPGA. The first approach is based on prevention of errors when SEUs cause bit flips either in the configuration memory, data memory or combinational paths. The technique to be used is Xilinx XTMR [3]. This technique has several advantages when compared with traditional TMR techniques, and also shortens development time because redundancy is automatically managed by the Xilinx TMRTool.

Traditional TMR does not protect against SEUs in voting logic or against Single-Event Transients (SETs), and does not lend itself well to the reconfigurable features of Xilinx FPGAs. Unlike traditional TMR, the XTMR approach involves:

- Triplicating all inputs including clocks and combinational logic,
- Triplicating feedback logic and inserting majority voters on feedback paths,
- Triplicating all outputs, using minority voters to detect and disable incorrect output paths.

The other major difference between traditional TMR approaches and the XTMR technique is that the redundant domains converge on the printed circuit board. If an upset occurs somewhere in the design, one of the redundant design domains will behave

differently from the others. The output voter for that domain will detect that its domain is behaving differently, and will place its pin in a high impedance state. The other two domains will continue to operate correctly, driving the correct output off the chip. If a voter is upset, the worst it can do is disable the output of a domain that is behaving correctly. As with the first scenario, the other domains will continue to operate correctly, driving the correct output off the chip.

### SEU Correction

The second approach is meant to correct SEUs in the configuration memory. Scrubbing [2] will be used to avoid XTMR becoming useless because of the accumulation of bit-flips in the configuration memory. This technique uses partial run-time reconfiguration to continuously re-write the FPGA configuration. If any bit-flip has occurred, it will be solved when the bitstream is updated in the next reconfiguration cycle. A complete study has been performed in order to adjust the frequency of the reconfiguration, see section 5.

Unlike any other previous approach [7][8], we have decided to include the scrubbing module inside the FPGA, as part of the SoC. The module will be implemented as a custom peripheral, directly attached to the processor's bus and connected to the Internal Configuration Access Port (ICAP). This architecture provides two major advantages over previous approaches:

- Hardware is simplified, because an external reconfiguration controller is no longer needed. Since the scrubbing module is connected to the SoC bus, the processor's non-volatile memory (Flash or EEPROM) may be also used to keep the scrubbing bitstream.
- A door is opened to a novel on-board dynamic reconfiguration. As the proposed architecture already offers self-reconfiguration capabilities, new bitstreams could be loaded with a telecommand from Earth in order to correct faulty/outdated designs.

There is however a drawback in the proposed approach, it is possible that a SEU hits the FPGA internal configuration logic, leaving the ICAP unusable. This is nevertheless a problem existing too in the designs using an external scrubbing controller. The solution is using a external FPGA watchdog that will be fired it the problem is detected, for example by reading unexpected data from a well-known configuration register. FPGA-based space systems usually provide external watchdogs, so this solution should not imply an increase in the complexity of the system.

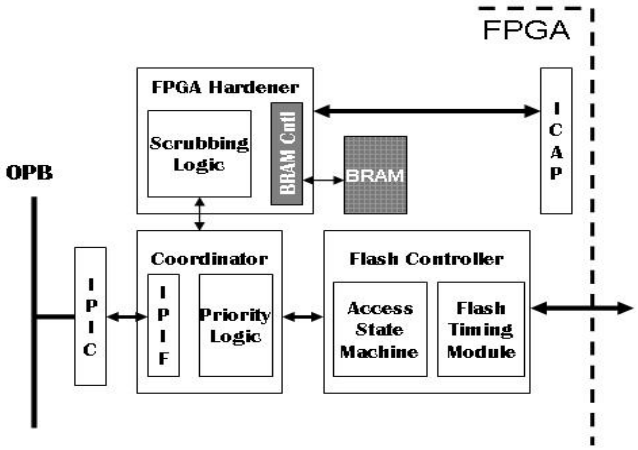


**Fig 1.** FPGA Hardener and Flash Controller modules.

### SYSTEM ARCHITECTURE

A complete SoC architecture has been designed to support a typical On-Board Data Handling (OBDH) functionality. This system will be based on a MicroBlaze soft-processor, due to its easy integration with Xilinx FPGAs and its good area-performance ratio. Attached to it, the whole set of typical peripherals and interfaces needed by most On-Board Computers (OBC) will be included, such as MIL-STD-1553 Bus Controller, RS-422, timers, interrupt controllers, etc. The new built-in scrubbing IP Core, so called "FPGA Hardener", is described in subsection 4.1.

### Built-in FPGA Hardener

The FPGA Hardener is a custom IP Core that will access flash memory to read the configuration bitstream, and then re-write frame to frame the FPGA configuration using the Internal Configuration Access Port. This process will assure the FPGA a good performance against SEU, correcting any possible bit-flip since the last scrubbing cycle.

Configuration bitstreams for Xilinx FPGAs are organized in frames of several thousand bits, 7872 in the case of a Virtex-II XQR2V6000. The minimum portion of bitstream that may be reconfigured is one frame. BlockRAM inside the FPGA Hardener will be used as an intermediate buffer to store frames before being sent to the ICAP (see Fig. 1). Since Virtex-II BRAMs have 18Kbits, they have enough space for storing 2.29 frames of a XQR2V6000

device. Therefore, only one BRAM will be needed to implement this intermediate buffer.

The FPGA Hardener will be directly connected the coordinator block, which is in charge of sharing the external Flash memory between the scrubbing module and the processor OPB bus.

## RECONFIGURATION CYCLE

It is very important to come up with the minimum reconfiguration frequency in order to minimize the possibility that there are two bit flips inside configuration memory at the same time. To be able to figure out this number we need to situate our system on a real space mission, so we can make a concrete radiation environment study. Taking into account the results of the radiation campaigns performed by the SEE Consortium members [7], CREME96 simulator has been used to adapt the Virtex-II characterization to a typical five-year Low Earth Orbit (LEO) space mission. Table 1 shows the Direct Ionization (Heavy Ions) SEU rate simulation results. The numbers have been obtained considering that the Virtex XQR2V6000 has 16,395,508 configuration bits. Table 2 shows the proton-induced SEU rate calculation, SEUs produced by nuclear recoils. After applying CREME96 to the Virtex-II SEU characterization on a real space orbit, we have found that we must foreseen 6.394 SEU/device/day, see Table 3.

Table 4. SEU rate of XQR2V6000, from data based on heavy ions irradiations at TAM facility

| SEEs/bit/sec | /bit/day | */device/day* |
|---|---|---|
| $1.933 \cdot 10^{-12}$ | $3.169 \cdot 10^{-5}$ | *2.739* |

Table 5. SEU rate of XQR2V6000, from data based on proton irradiations at UCD facility

| SEEs/bit/sec | /bit/day | */device/day* |
|---|---|---|
| $2.676 \cdot 10^{-12}$ | $4.388 \cdot 10^{-5}$ | *3.791* |

Table 6. Total SEU rates with Heavy Ions and Protons using TAM and UCD data

| SEEs/bit/sec | /bit/day | */device/day* |
|---|---|---|
| $4.6 \cdot 10^{-12}$ | $3.9 \cdot 10^{-7}$ | *6.394* |

In order to get the minimum scrubbing rate, Xilinx recommends scrubbing at least at a rate ten times higher than the SEU rate. For the proposed orbit, the maximum scrubbing cycle will be 24 hours divided by 63.94 (ten times the expected SEU rate), that is, 22.52 minutes

On the other hand, assuming that a typical read access to the Flash memory is done in 50ns with a data bus of 8 bits, and that the XQR2V6000 has a total number of 16,395,508 configuration bits, then the time to completely reconfigure the device will be 0.1025 seconds. In order for the processor to be able to access the Flash memory without excessive wait states, we do not advise to use it for reconfiguration more than the ten percent (10%) of the time. Therefore, we do not recommend a faster scrubbing cycle than 1.025 seconds.

Table 7. Maximum and minimum scrubbing cycles

| | |
|---|---|
| Maximum Scrubbing cycle | *22.52 minutes* |
| *Minimum Scrubbing cycle* | *1.025 seconds* |

## CONCLUSION

In this paper, a novel approach based on the XTMR tool and the use of self-reconfiguration is proposed to develop radiation hardened SoCs based on Xilinx FPGAs. These two techniques are combined together to enable a reliable operation of a FPGA-based SoCs in space applications. A full on-board computer could be implemented on a single FPGA device, significantly reducing cost, space and power requirements. The architecture proposed to implement these systems has been described, as well as the details of the peripheral in charge of the self-reconfiguration required to mitigate SEUs in the FPGA configuration memory

Although the main purpose of the architecture is to provide a reliable operation, there is an interesting side-effect of self-reconfiguration. Reconfiguration enables hardware updates, thus permitting many different problems such as design errors, modified algorithms or compatibility issues to be remotely solved.

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